Sort ASIC Design

Finds the 4 largest of thirty-two values

Sorts electrons by rank

Finds the 4 largest E_T from sixteen 4 x 4 regions

Inputs

Eight 10-bit ECL inputs @ 160 MHz. Four cycles to read in thirty-two values

Each input has 5 bits added:

3: which input of eight

2: which cycle of four

Outputs

Four 15-bit ECL outputs are produced @ 40 MHz

Five bits added to each 10-bit result:

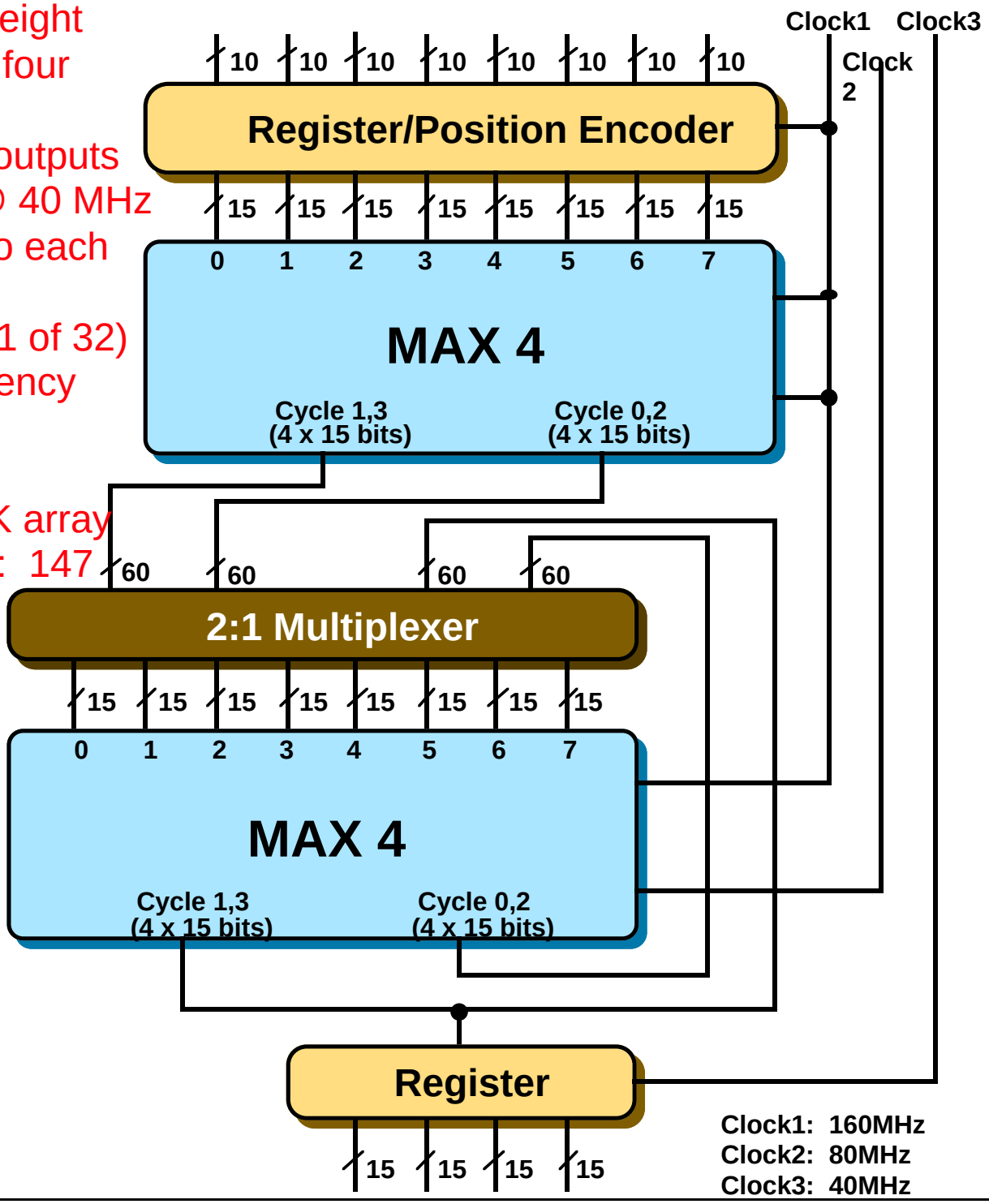
tower address (1 of 32)

Four crossing latency

Package:

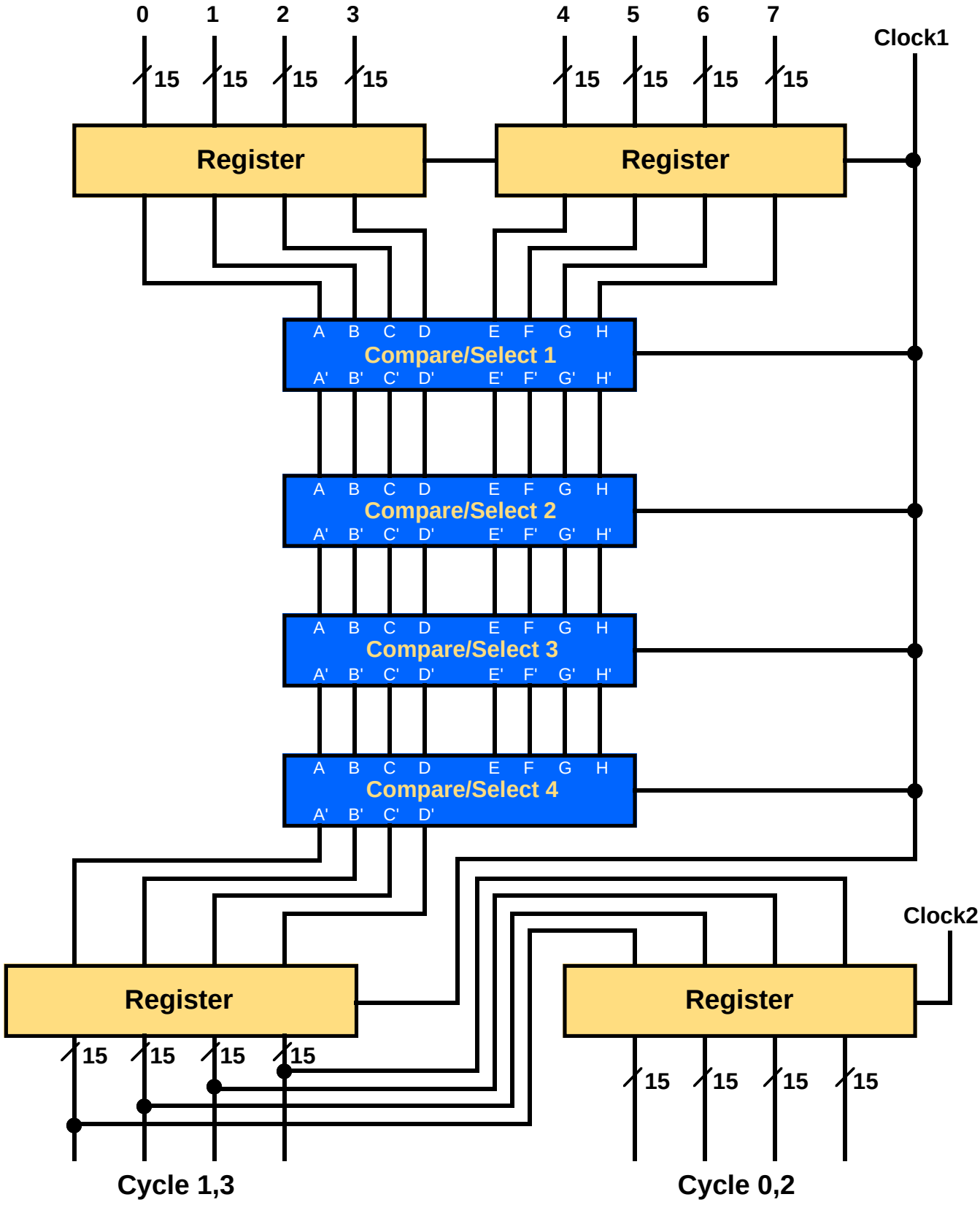
Vitesse's FX100K array

Signal Pin Count: 147

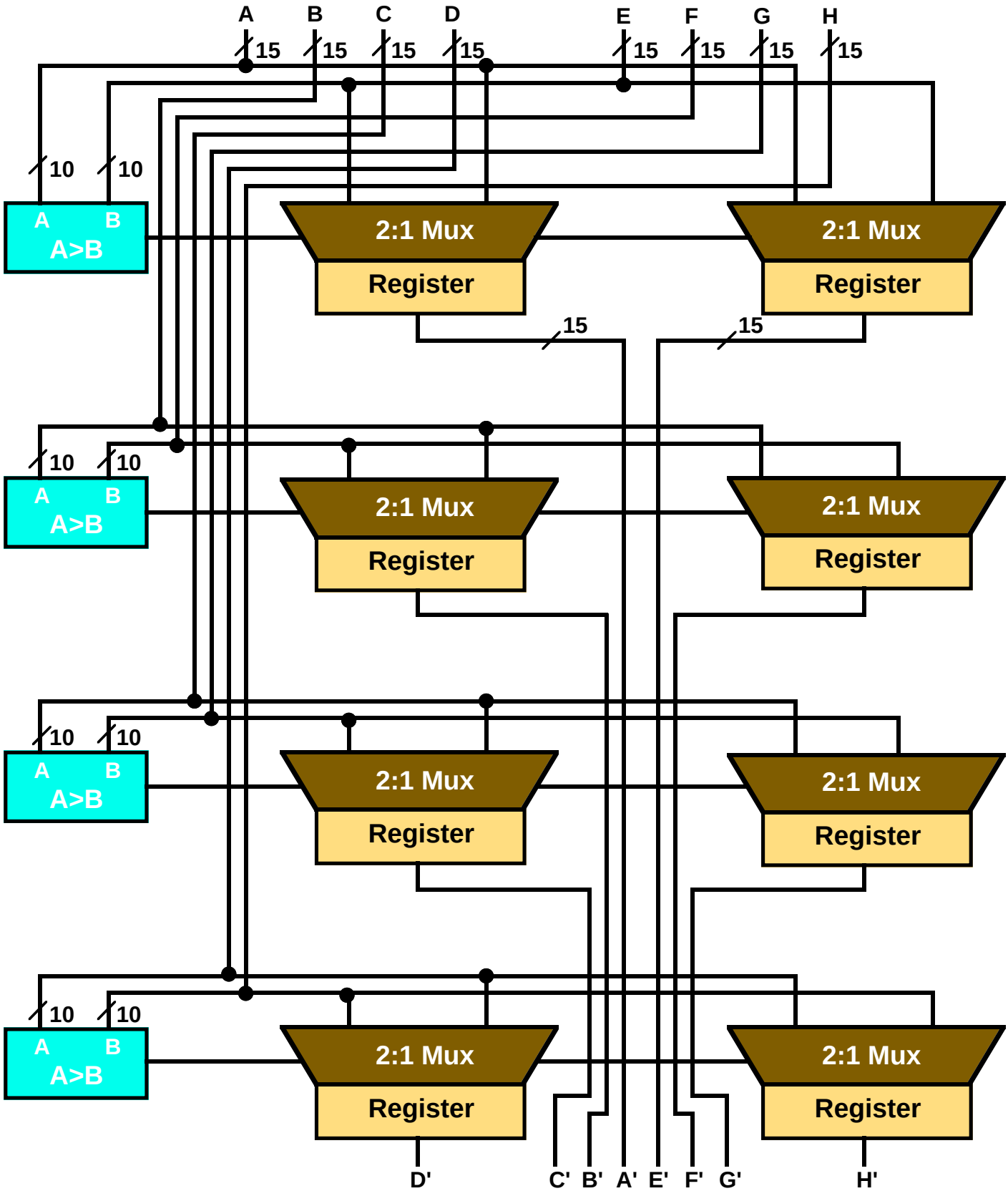


- J. Lackey

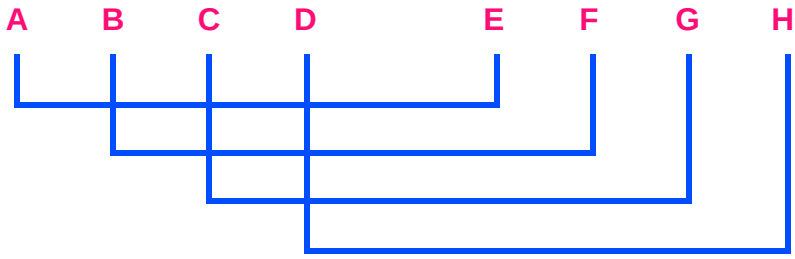
Max 4 - Sort ASIC



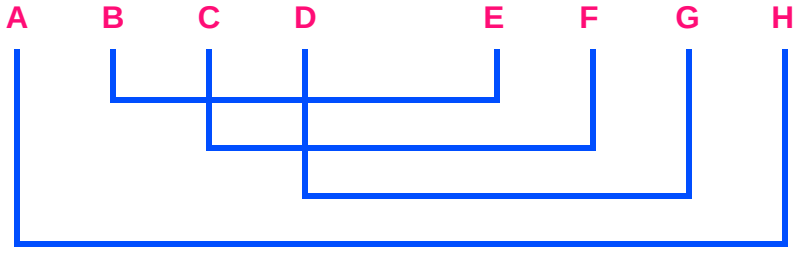
Compare/Select 1 - Sort ASIC



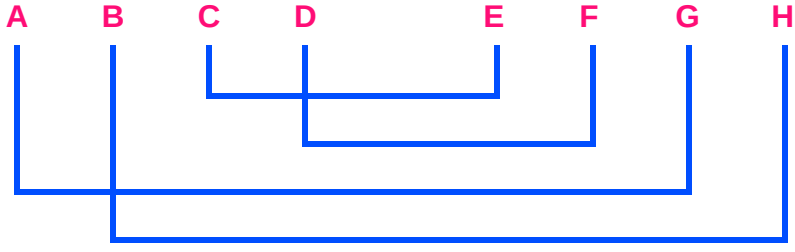
Compare Patterns - Sort ASIC



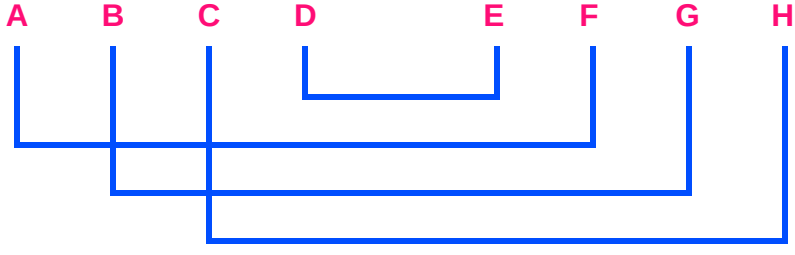
Compare/Select 1



Compare/Select 2



Compare/Select 3



Compare/Select 4