The CMS Global Calorimeter Trigger

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LEB-Conference 1998, Roma

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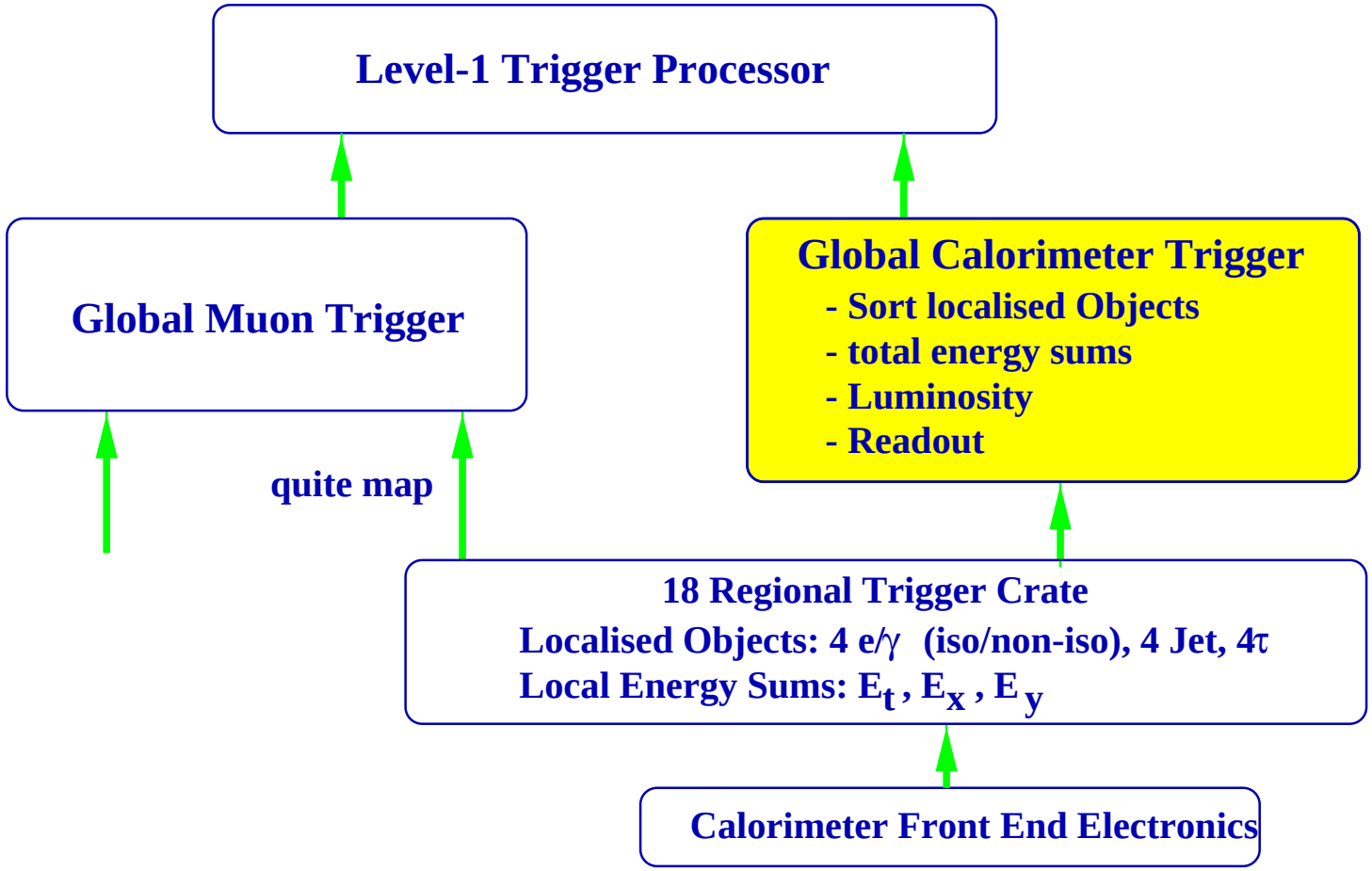
Trigger Processing Overview



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Input to the Global Calorimeter Trigger

Jet Summary Card the Interface to the GCT:

- Determain the 4 highest ranked Objects

  in an (8*2) $(\eta*\phi)$ range

  Objects: ⟶ isolated- e/γ , unisolated-e/γ ,

  Jets, Tau

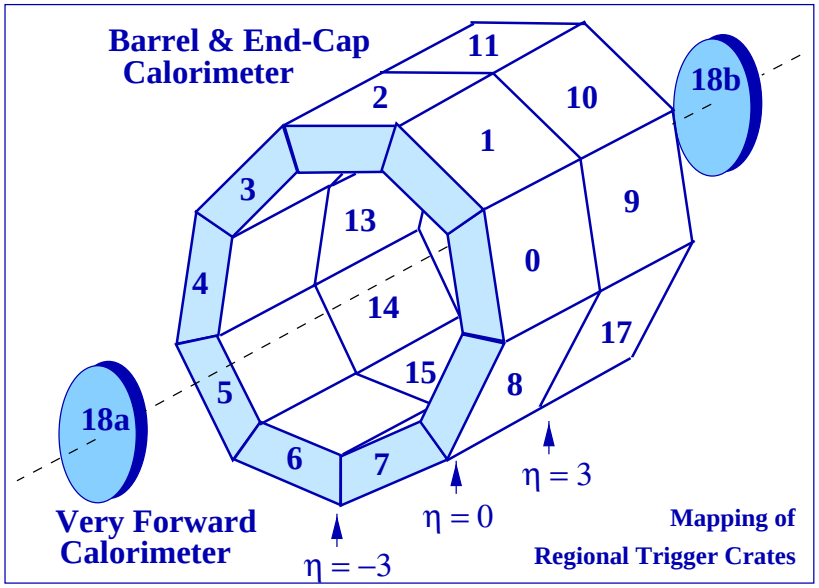
  Format: 6 bit rank + 4 bit location @ 160MHz

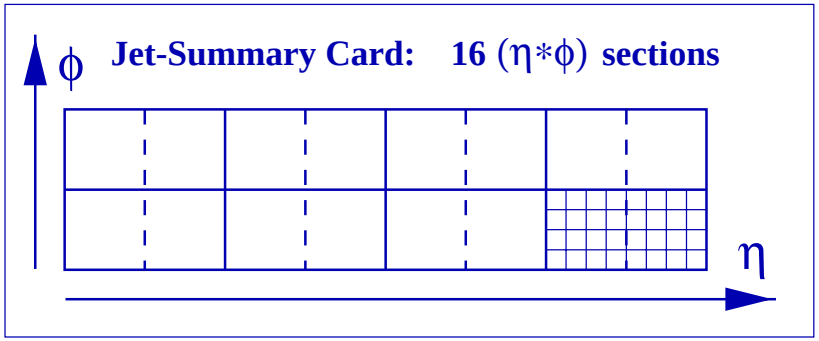
- Calculate E_t , E_X , E_Y in same range

  Format: E_t 12 bit @ 40 MHz

  E_x , E_y 13 bit @ 40 MHz

Special Interface to Very Forward Regions





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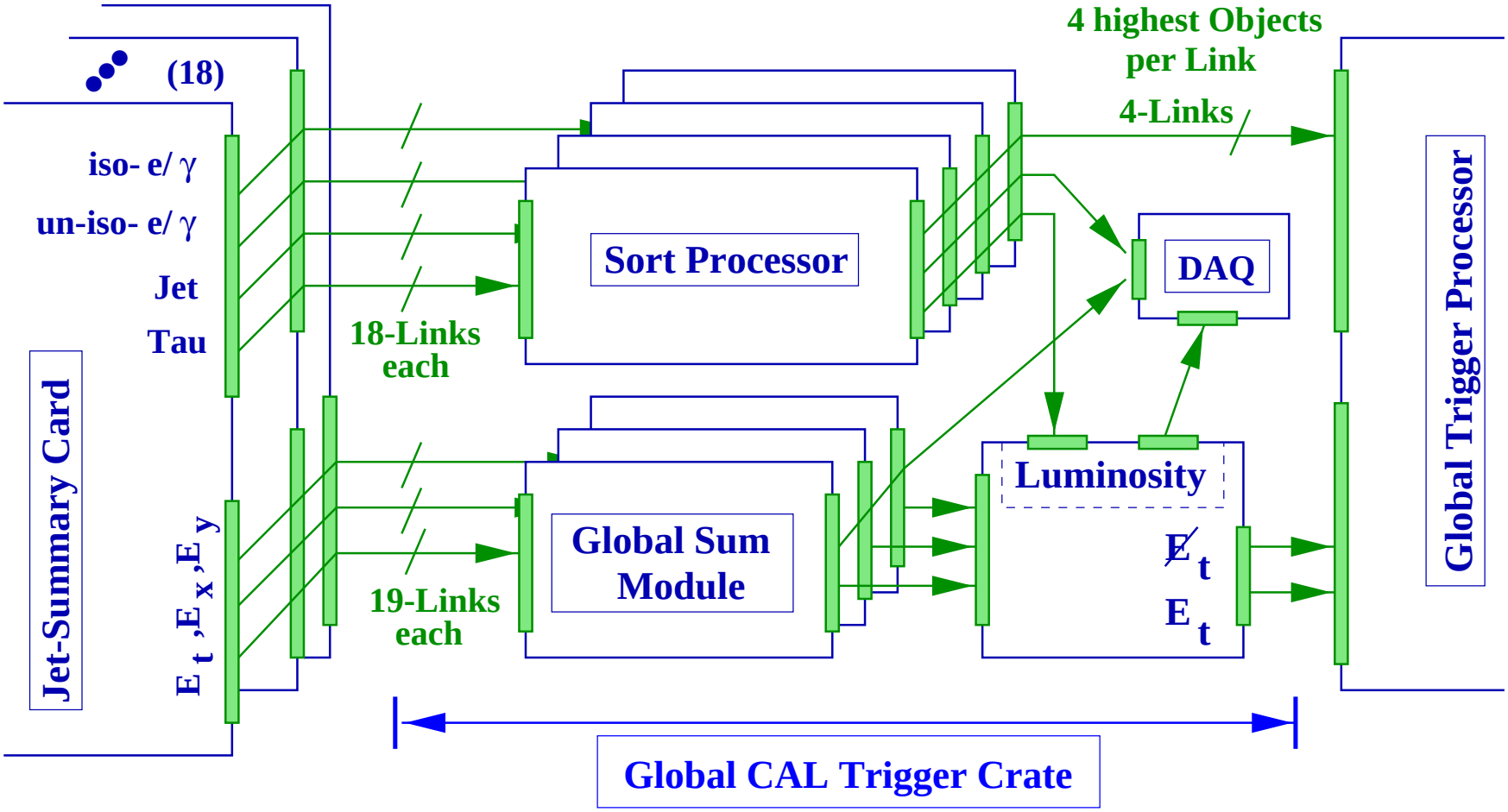
Global Calorimeter Trigger Block Diagramm



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Link Issues

- GCT should not restrict the Regional Crate timing (data rate of 160MHz)
- Use 40 MHz differential ECL Links for inter crate/module communication

  (No custom back plane)
- Use common Link design in regional and global trigger crate
- Use compact connector technology:

  - need 276(247) differential pairs input to Input-Sort-Module(Global-Sum-Module)

    (for instance CHAMP 0.8 -> 68 pairs; 4 cm high)
- Use integrated time DeMux (Wesley), and discrete time MUX

  - requires about a 100 discrete components for the receiver
- Use rear receiver modules to source out part of the receiver circuit

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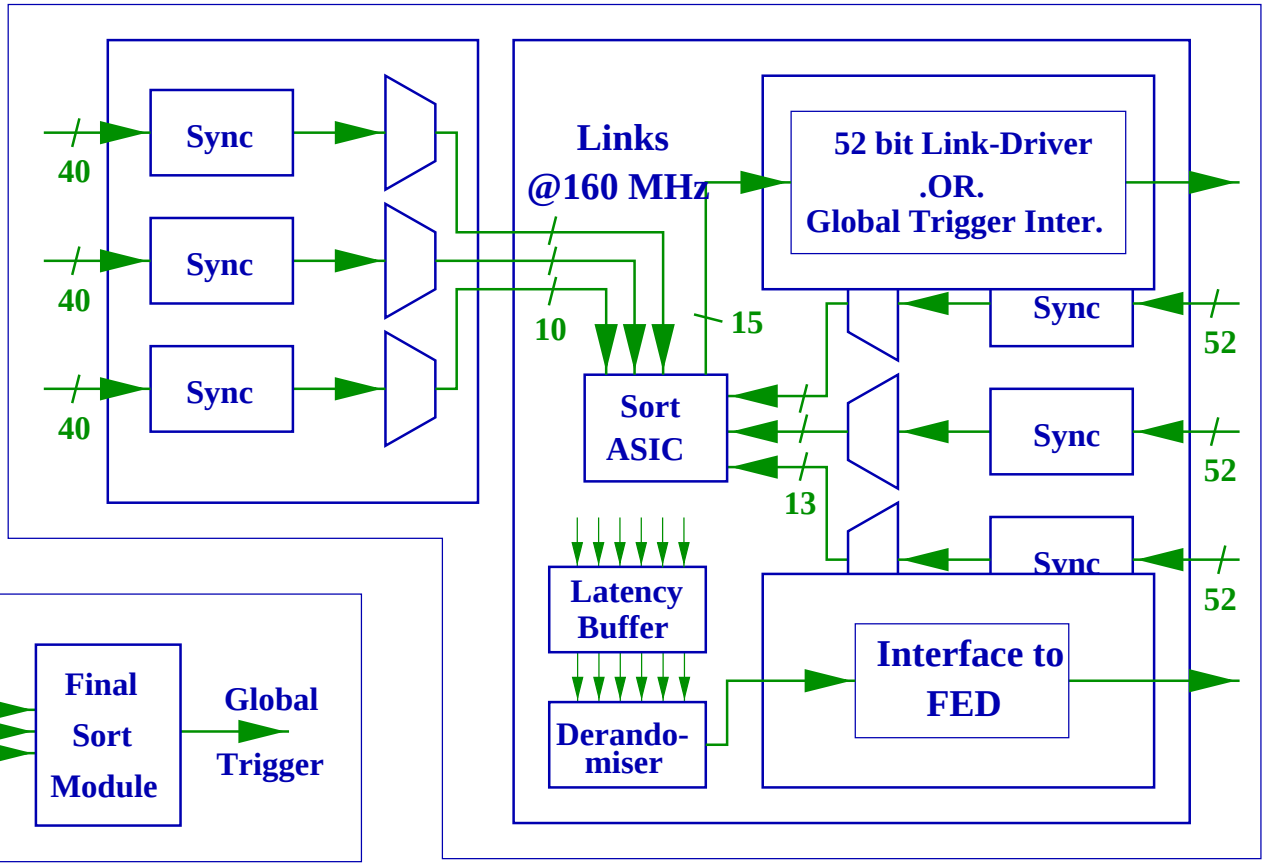
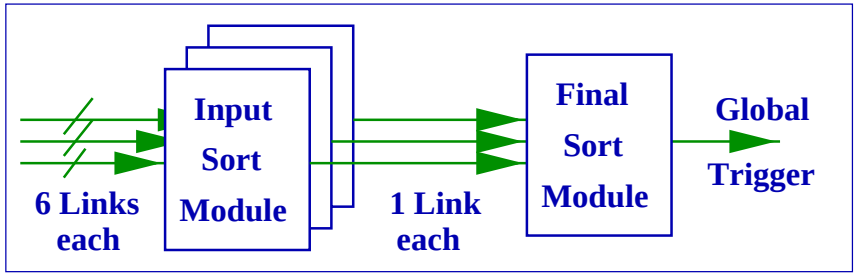
The GCT Sort Processor

- Use rear receiver Board

  for Input Sort Module
- Use Mezzanine Cards
  - Input Sort to Final Sort
  - Final Sort to Global Tr.
  - Sort to FED
- Record data from all Links





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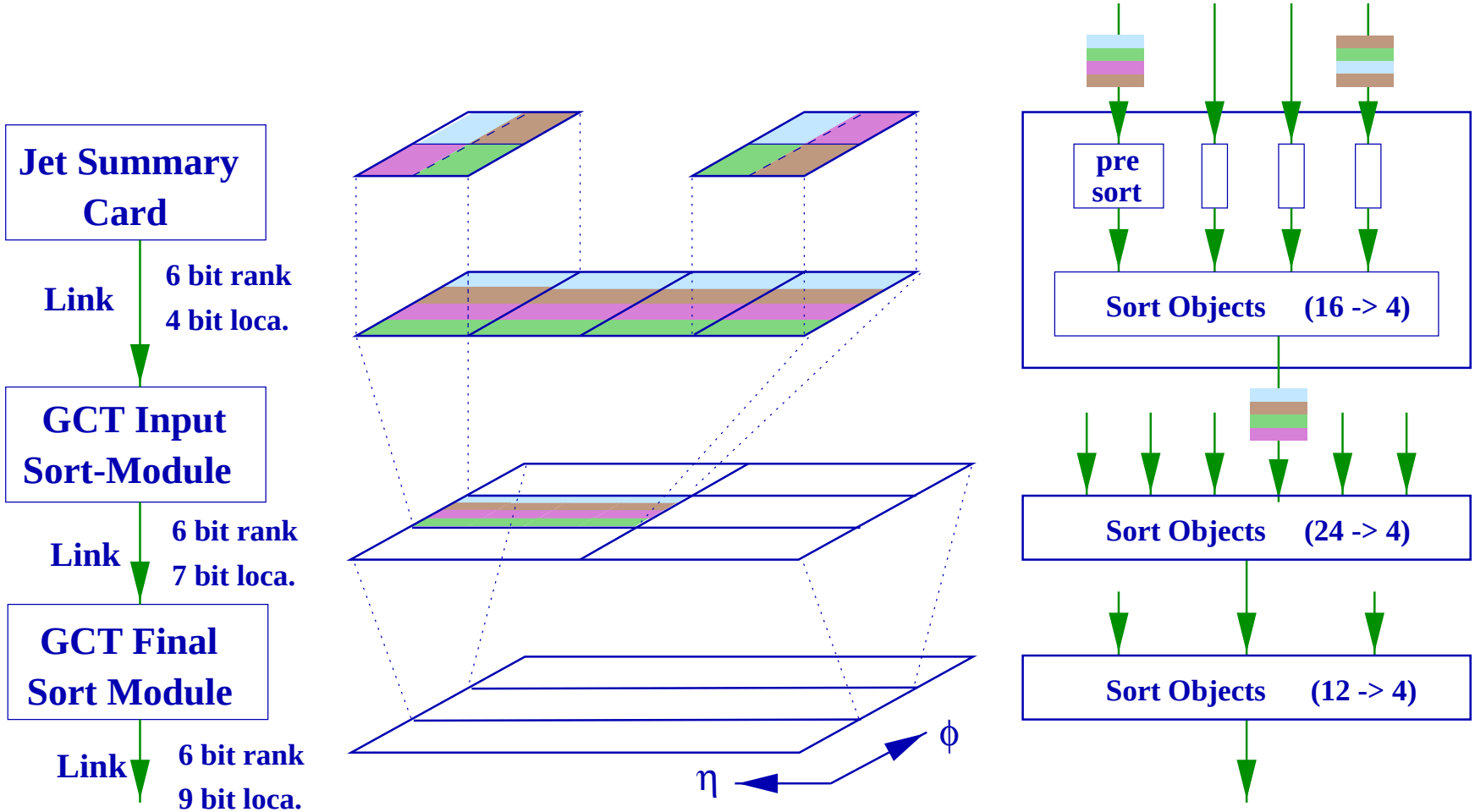
Sort Tree for Localised Objects



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Sort ASIC

- Use same Sort ASIC in all tree levels

  Configurations: (rank always 6 bit)

  a) 4 ranks; unsorted no location

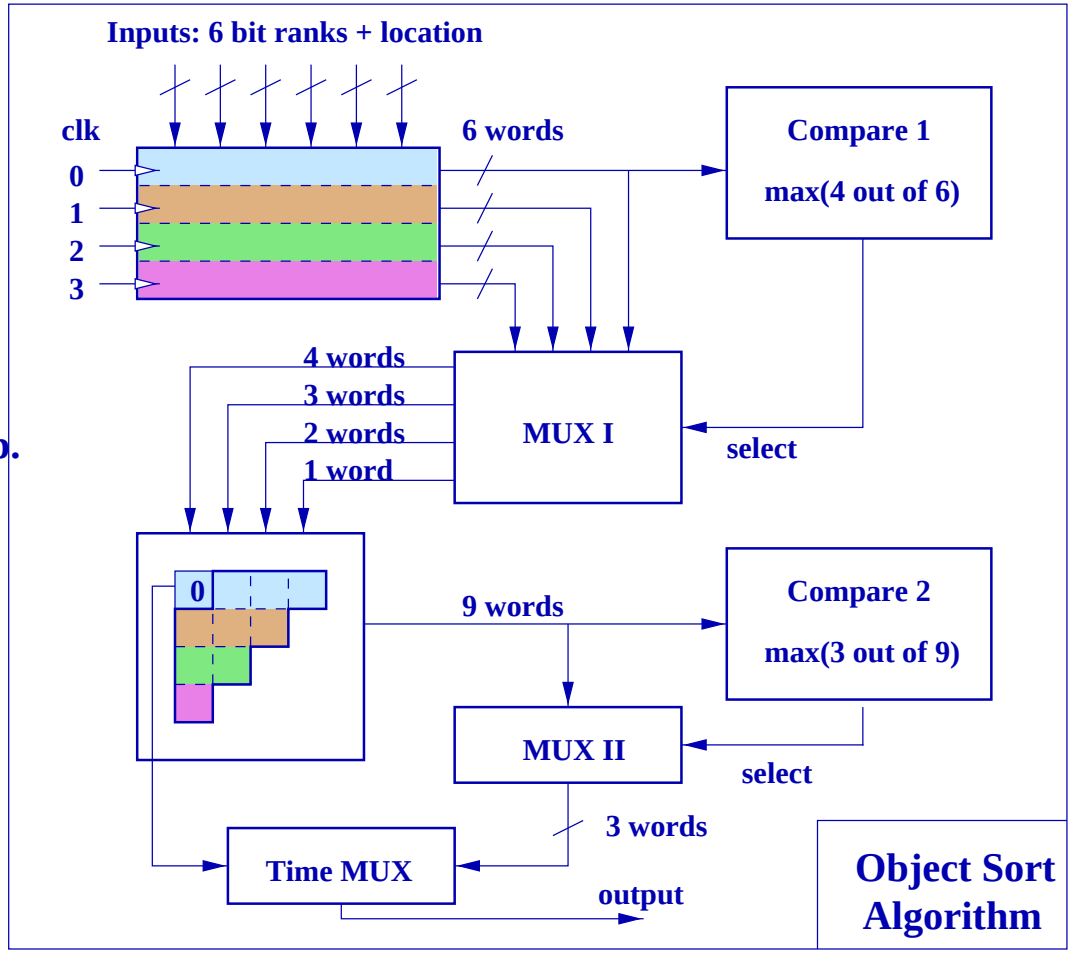
  b) 6 ranks; sorted 4 bit location

  c) 3 ranks; sorted 7 bit location

- Requires Pre-Sort unit for unsorted inp.
- Input/Output data ECL @160 MHz
- Boundary Scan
- Schematics design for I/O

  VHDL for the Object Sort (TTL)

- Latency: 50 nsec (2 BC)



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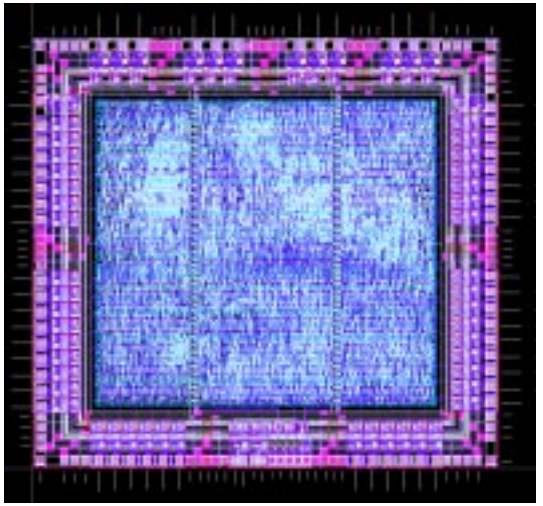
GCT Demonstrator Project

- **Design of Prototype Sort ASIC (manufactured 1997)**
  - **Object Sort for (32 -> 4)**
  - **4 Inputs (8 bit rank, 3 bit location) @160MHz**
  - **ECL I/O (Boundary Scan)**
  - **Schematic design**
  - **Funtion successfully tested @50MHz**



- **160 MHz Sort ASIC Test System**
  - **Sort ASIC Test Module: 4 random pattern generator + Sort Asic**
    + (160MHz -> 40MHz) DeMUX + 160MHz clk generator (RAL)
  - **64 bit ECL Data Recorder/Source, Readout via custom fieldbus (Bristol)**
  - **All PCBs made; Assembly completed in Sept.; Test in Oct. & Nov.**
  - **Fieldbus firmware design almost complete, driver software complete**

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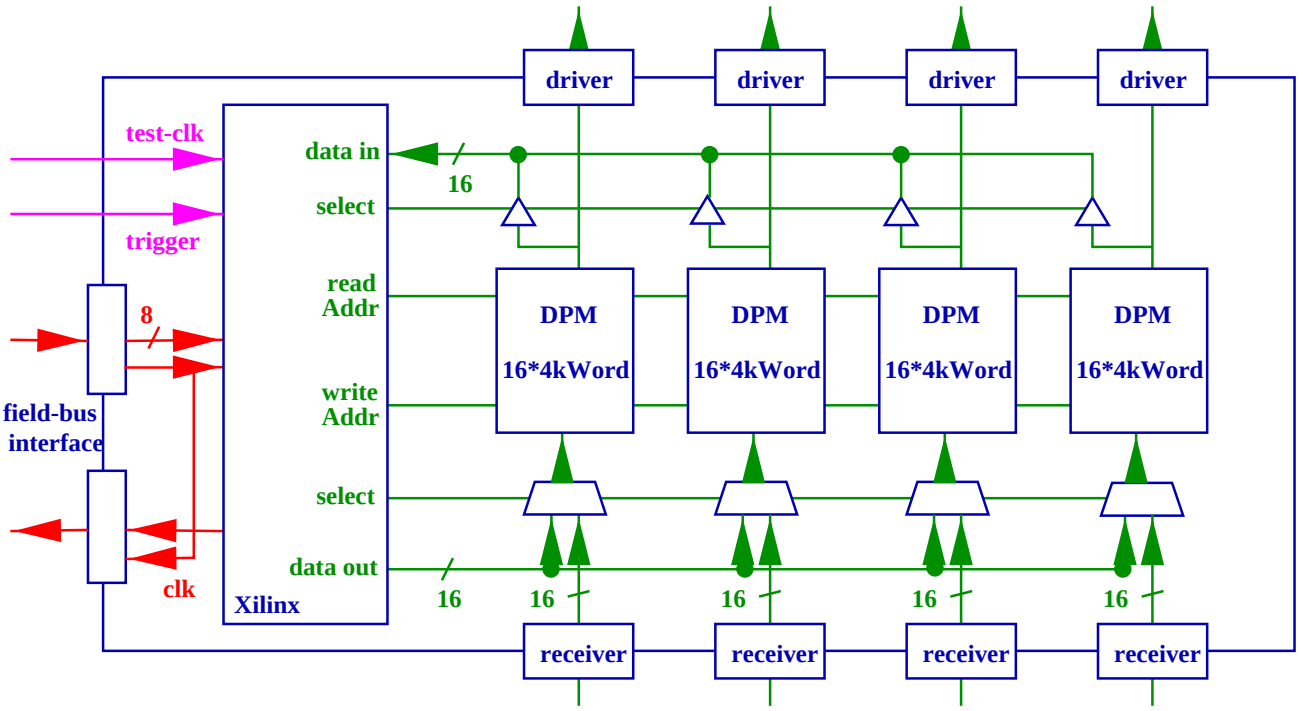
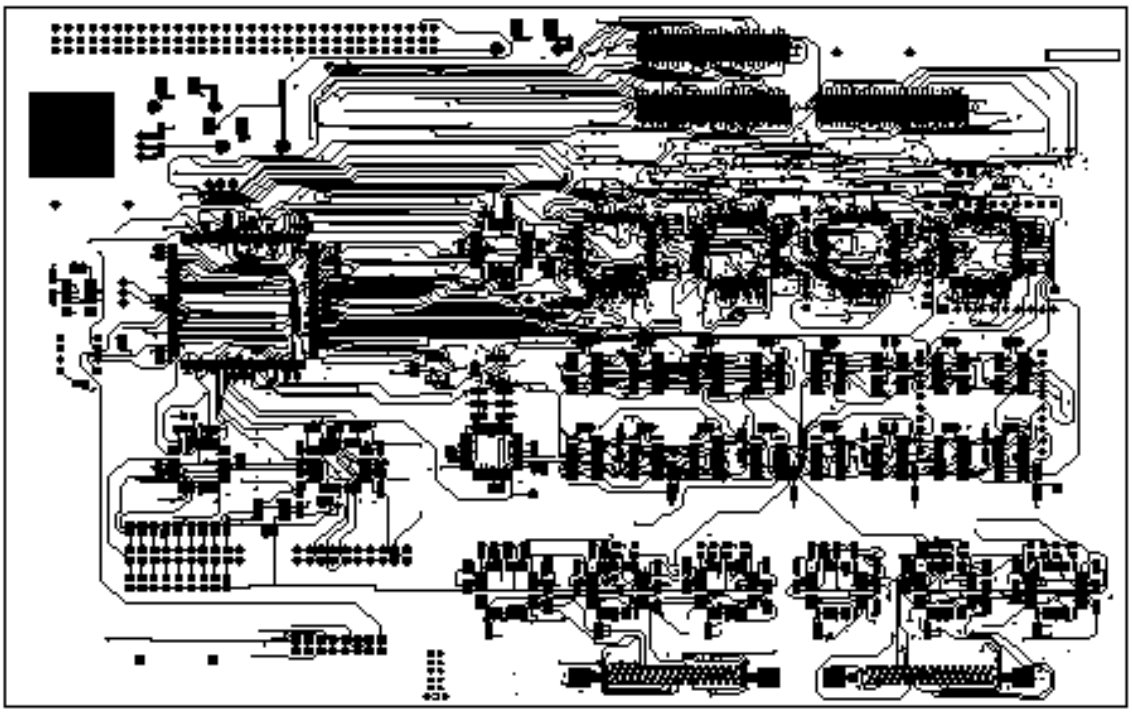
Memory Module





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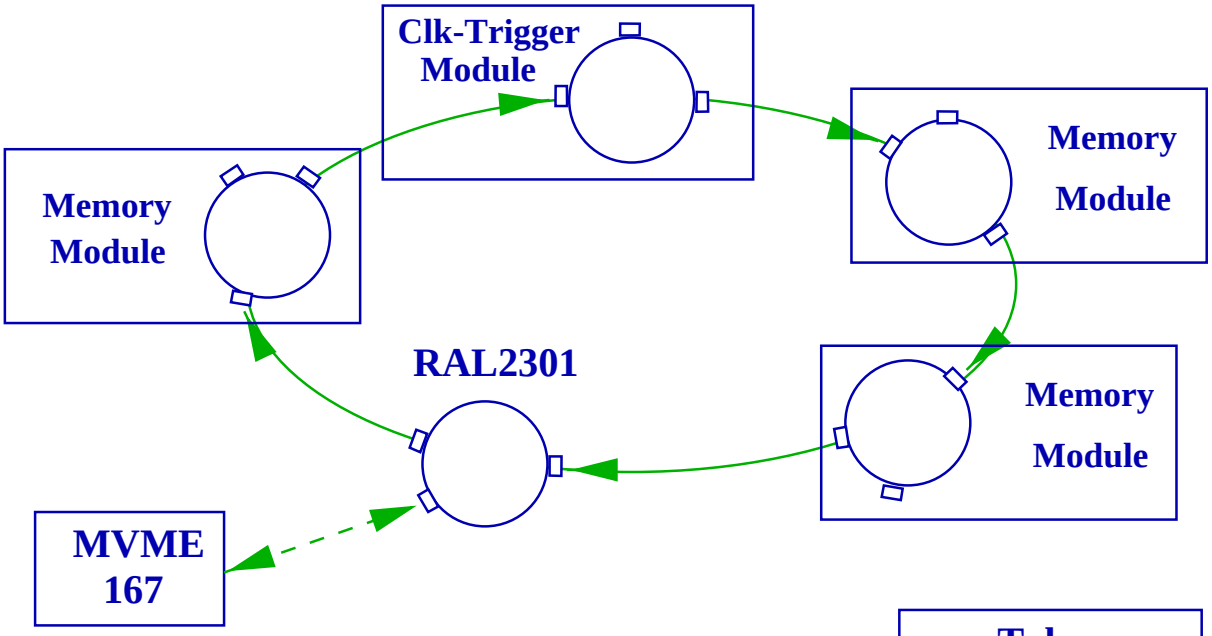
Summary

- Presentation of the Global Calorimeter Trigger Sort Processor
- Discussion of the Link between Regional and Global Calorimeter Trigger
- Description of the Object Sort Algorithm
- We have demonstrated that we are able to design the required ASIC
- A 160MHz Sort ASIC test system has been build.

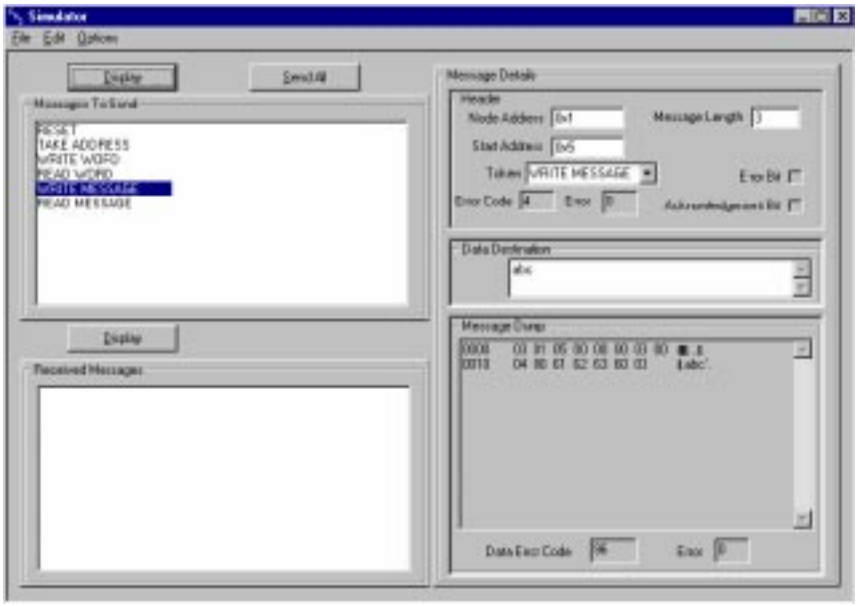
  The high speed Sort ASIC test will be completed end of the year

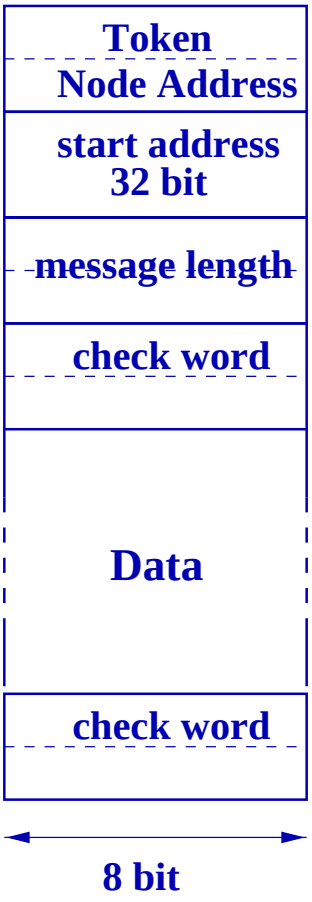
Fieldbus Design Overview



Tokens: Reset, Take-Addr, Read, Write

Clk-Speed: 40MHz





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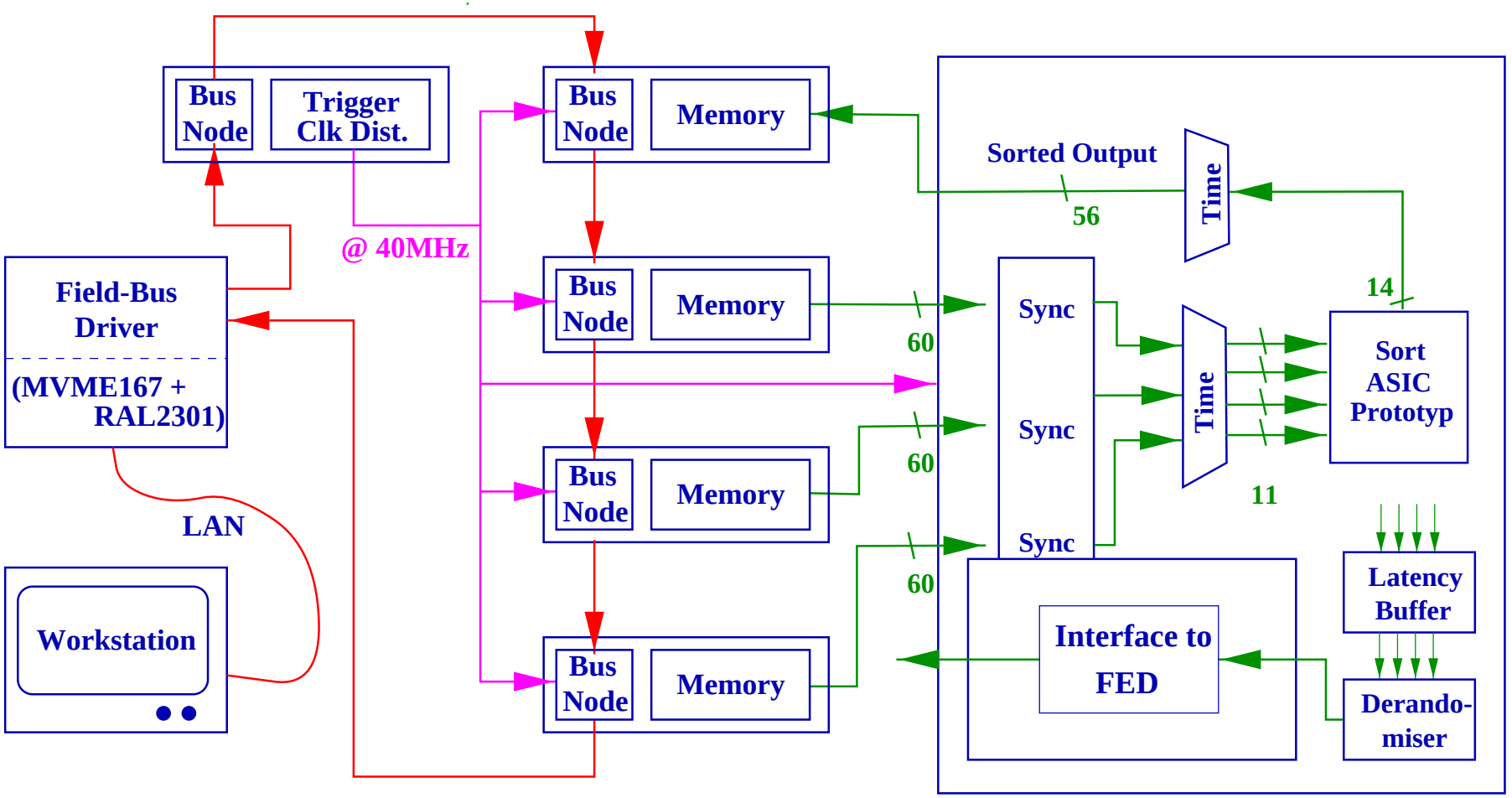
The Funtional Prototype (1999)



Next Milestones

- **Complete initial Trigger Design (Nov 99)**
- **Complete sort ASIC prototype test (Dec 99)**
- **Start design of functional sort processor Prototype (Jan 99)**
- **Start design of final sort ASIC (Jun 99)**

  (requires freezing of all I/O interfaces)
- **Complete Prototype Design (Nov 99)**