SLINK : How to proceed?

- I) Put intellingence into transmitter card

  + full Slink compliance
  - additional cost
  -additional work + development

- II) Change specification (+ trivial change in hardware)

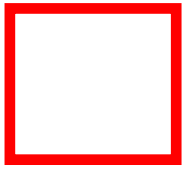
  + full SLINK compliance

  - Slink32 and Slink64 are slightly different (could be confusing)

  - probably disfavoured by E.van der Bij

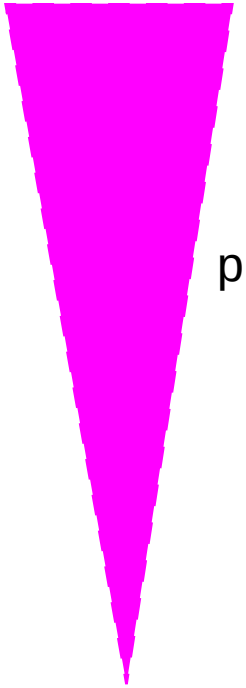
- III) Declare new specification for CMS

  + no problem with compliance etc
  - need to spread out the information (might confuse FED developers)

We decide to go for : 

Future Activities
a subselection of the last hardware meetings items

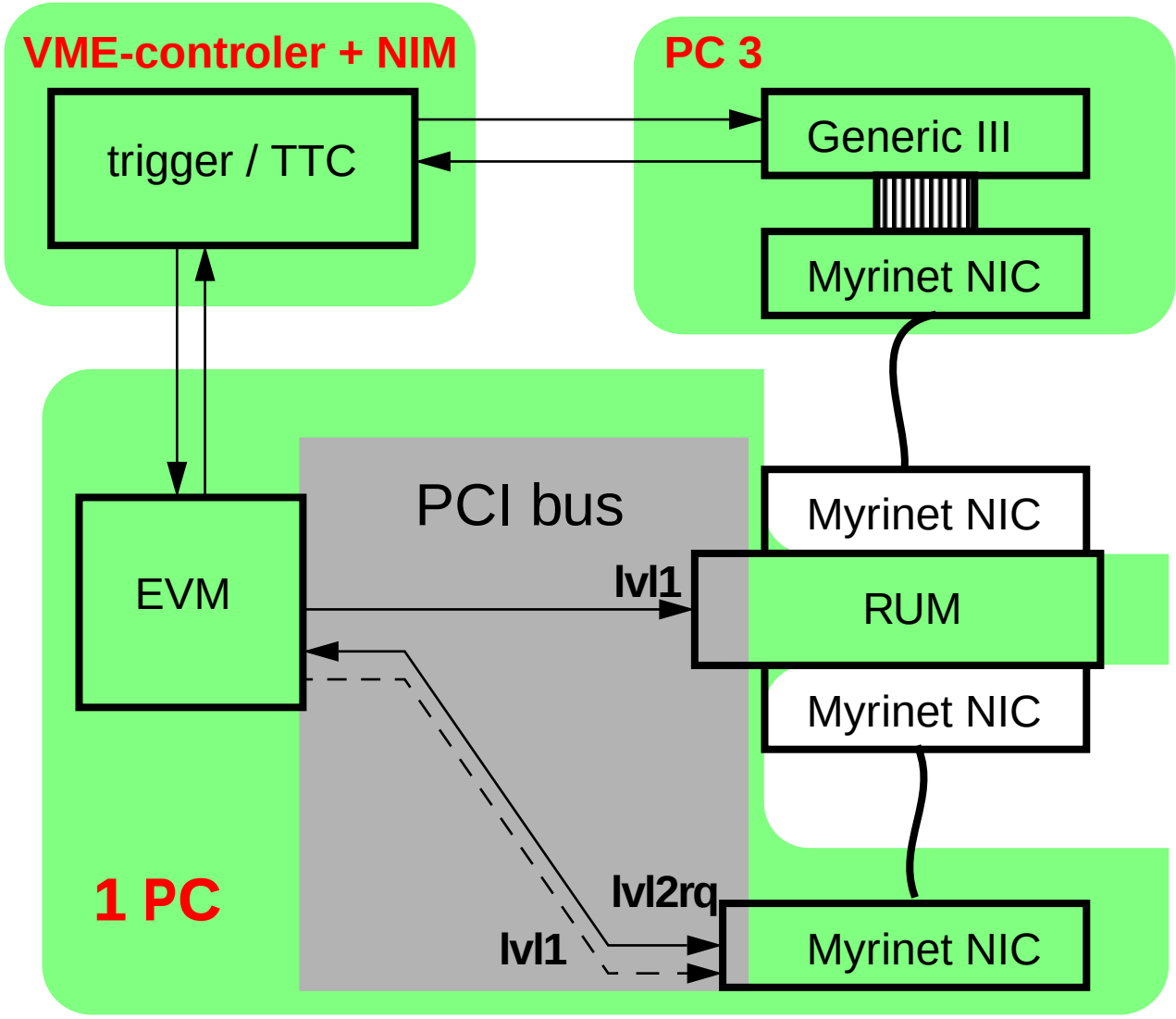
- Test benches for DAQ - System prototyping:
  - DAQ Column with Hardware RUM
  - DAQ Column with Software RUM
  - FRL prototyping
  - FED-builder prototyping



priority ?

- DAQ - KIT for outside groups
  - hardware : LVDS driver + GIII card
  - software : XDAQ based readout - kit

hardware Column



PC / software Column

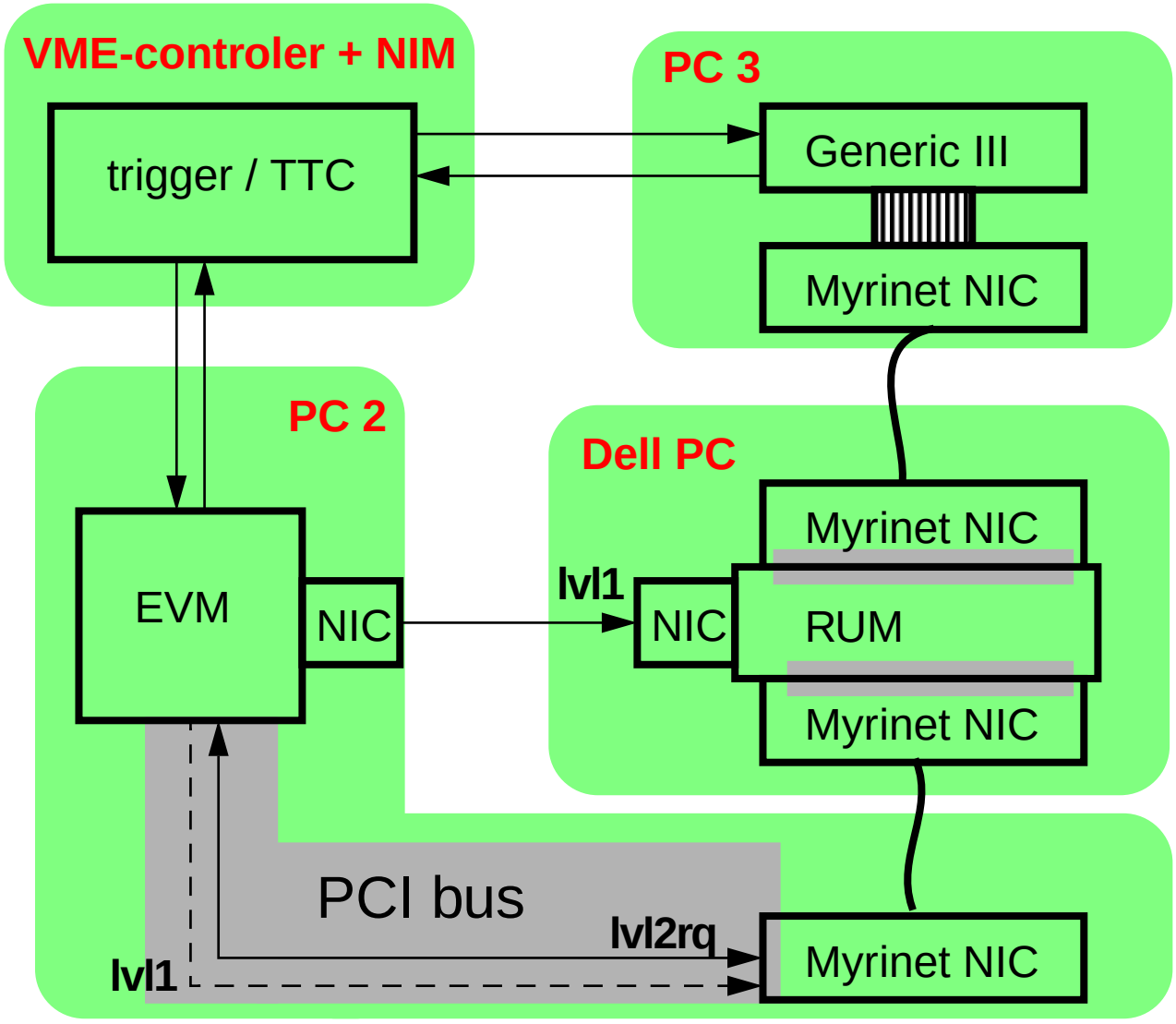


Table of Activities

H/S/F	activity	time	who?
Firmware	FED emulator (GIII)	1 week	
	FPGA RUI (GIII)	2 months	
	FRL emulator (GIII)	2 months	
	Glob.Trg. Proc emulator (GIII)	2 months	
Software	Control software for hardware	1 week / module	
	DAQ user toolkit with hardware access library	4-6 months + iterations	
	Software RUM (with DELL)	2 months	
	NIC as RUI / FED-Builder receiver	???	
	NIC as BU	???	
	NIC in RUO	done?	
	NIC as FRL output	???	

H/S/F	activity	time	who?
Hardware	Slink with intelligence in sender?	2 months	
	FED merging hardware (multi LVDS receiver)	3 weeks	
	TTCrx new setup	2 months	

Column PC / software

- RU Input
  - simplified scheme of Johannes and Luciano
  - feasable for Generic III
  - investigate if this is applicable to Myrinet card in order to build RU without custom hardware.
  - program Myrinet cards for buffer loaning at input