Readout Column Status

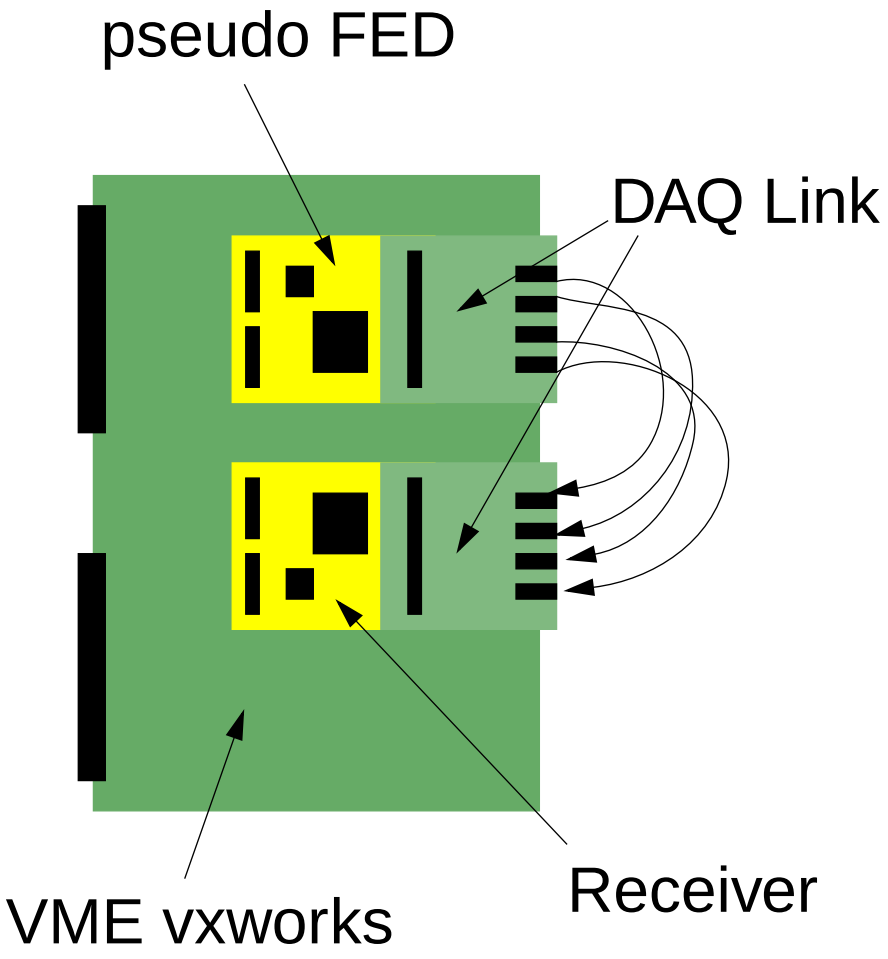
stage 1 status (february)

stage 2 status (june)

technicalities

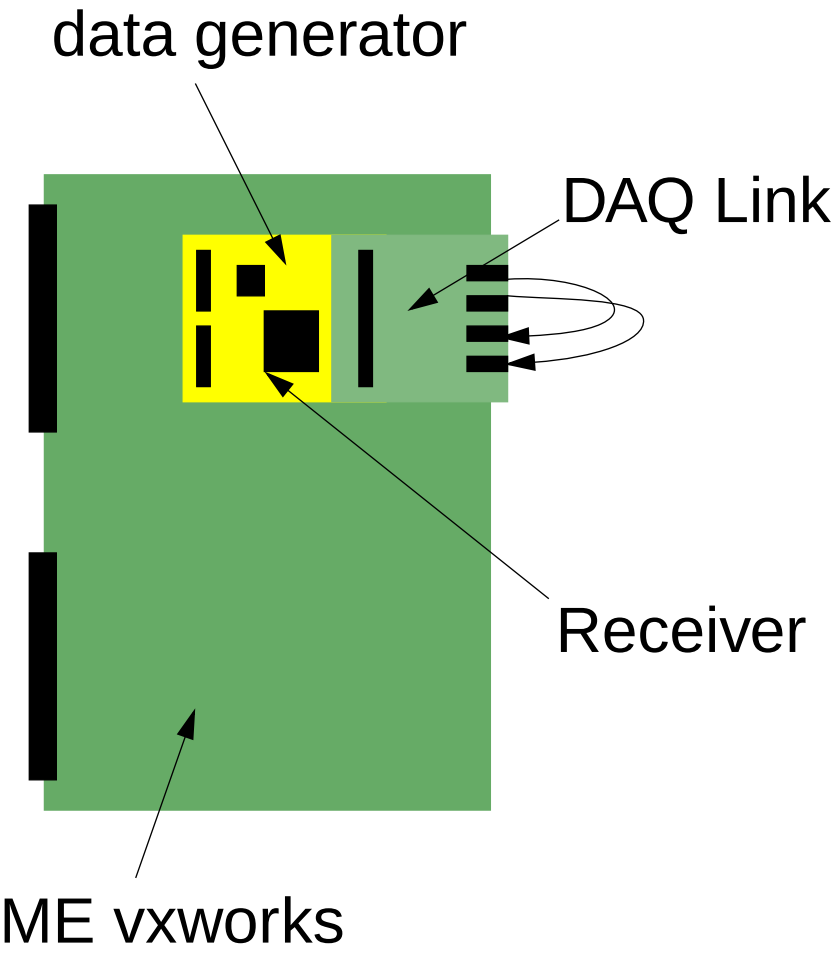
Stage 1: RUI - DAQ-link

- Purpose
  - data transfer over DAQ link
  - bandwidth of link
- Hardware
  - 2x generic II
  - 2x Siemens Link
  - 1x VME-processor with two PMC slots



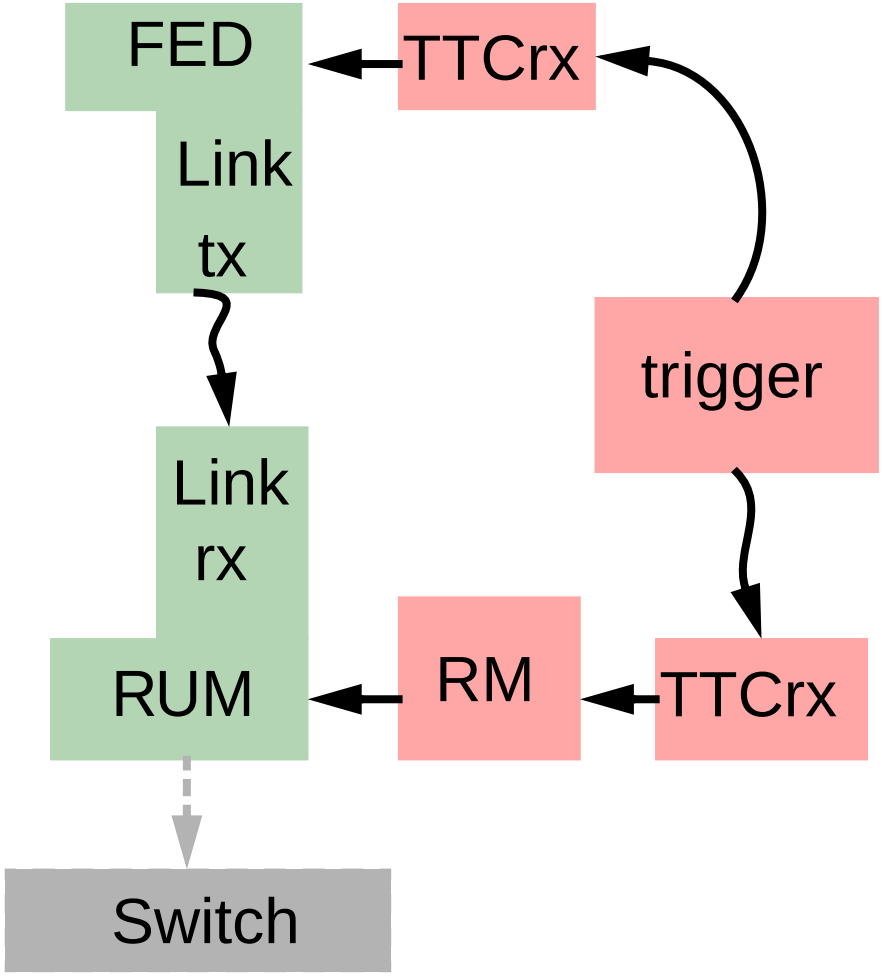
Current Status

- Hardware
  - 1x generic II + Link working
  - 1x generic II + Link under construction
  - !x VME processor with basic test software
- “Firmware” (FPGA code)
  - data generator **ok**
  - Vitess and Fifo “driver **ok**
  - readout memory **ok**
  - MMU **simulated**
  - DMA fpga -> memory **simulated**
- Software
  - simple test software in C **ok**
- Status
  - Principle proven, measurements tbd

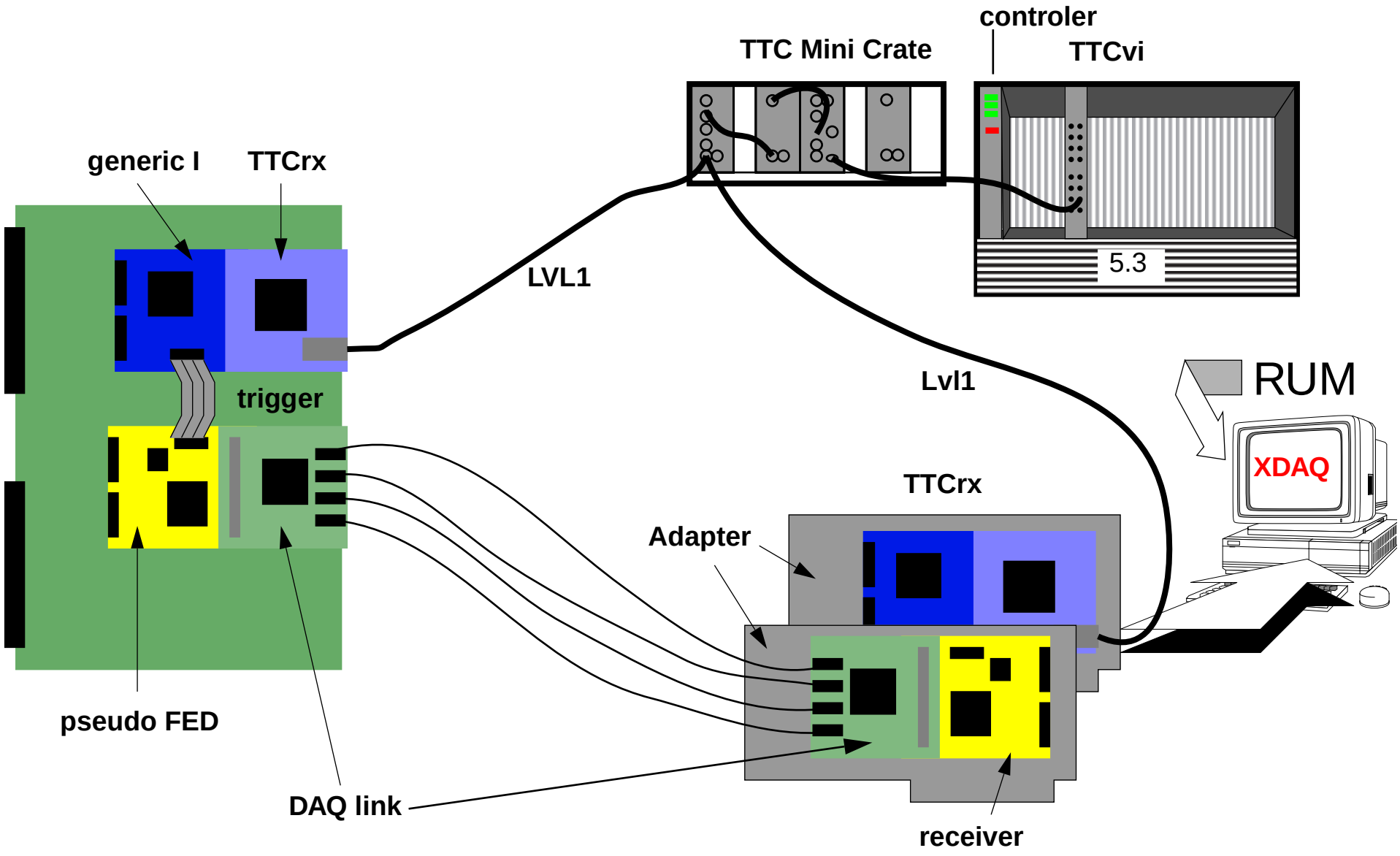


Stage 2 (june)

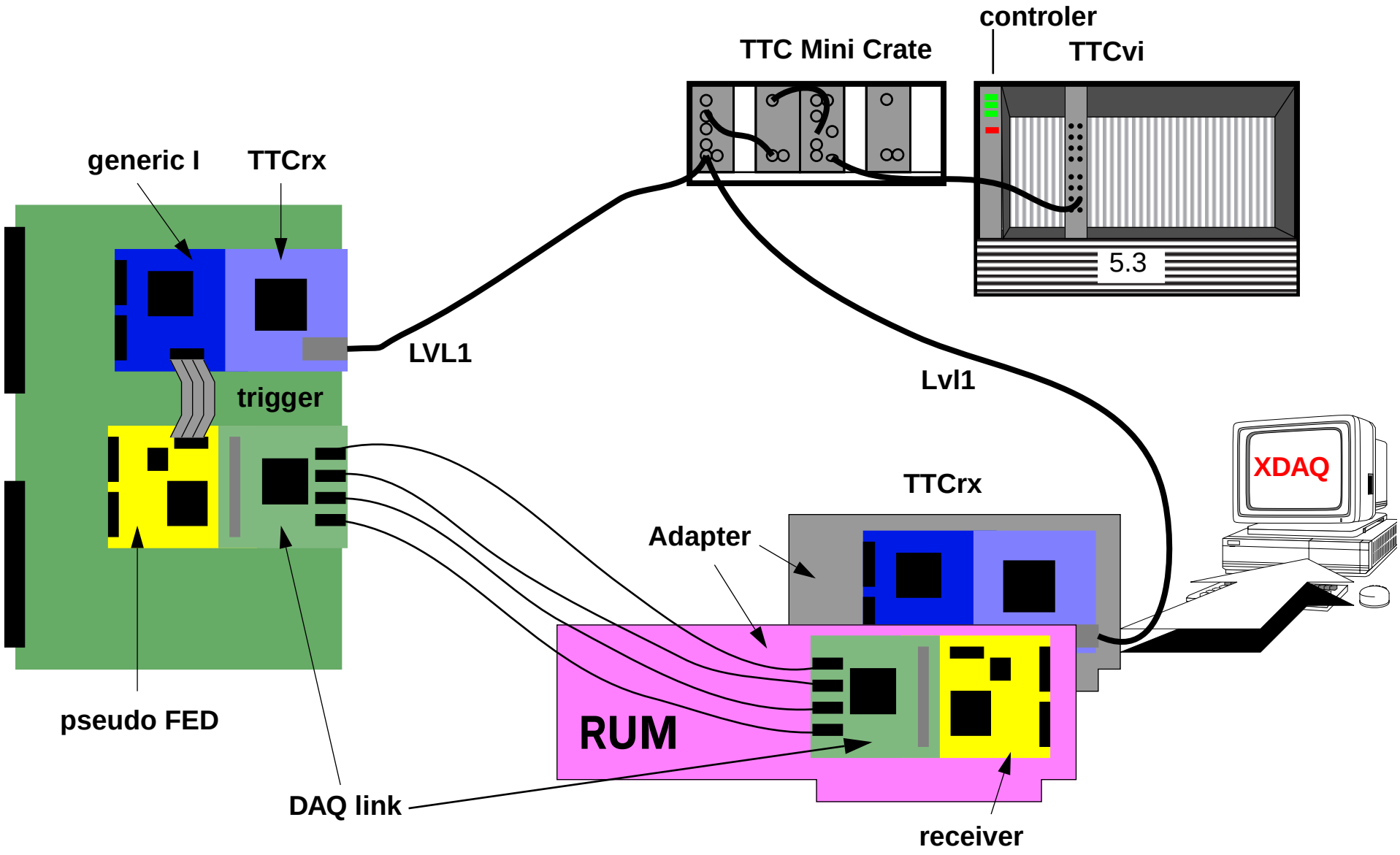
- Purpose
  - build a DAQ chain Pseudo-FED - RUM
  - demonstrate the concept
  - see for the first time bytes flowing between different building blocks
  - use software and hardware RUM
  - develop interface DAQ-Link RUM
  - identify bottlenecks in hard- and software
  - write results down into TDR
- NON-purpose
  - Performance and data throughput



Stage 2a : with software RUM

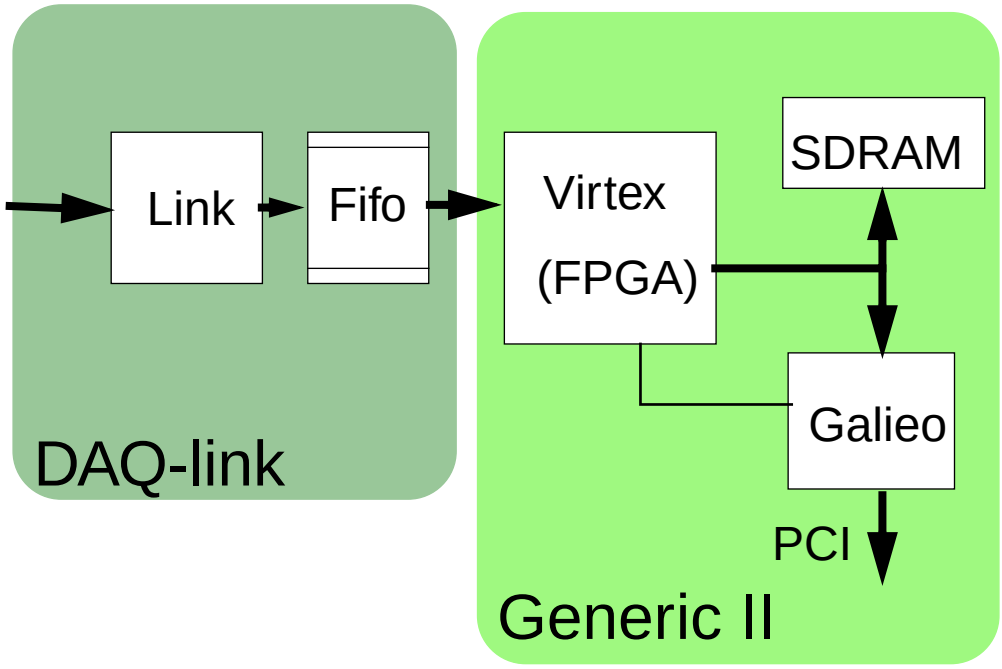


Stage 2b : with hardware RUM



DAQ-Link Hybrid

- Psudo FED / sender
  - receive triggers
  - generate dummy data
  - transfer them to the link
- Receiver / Interface to RUM
  - receive data from link in buffer fifo
  - DMA them to SDRAM
  - setup descriptors for RUM
  - interface to RUM (hardware / software)
- Status
  - Pseudo FED to be done
  - Receiver FPGA code exists (tested with Xilinx-Micky-Mouse simulator) for software RUM
    To be tested in Generic II

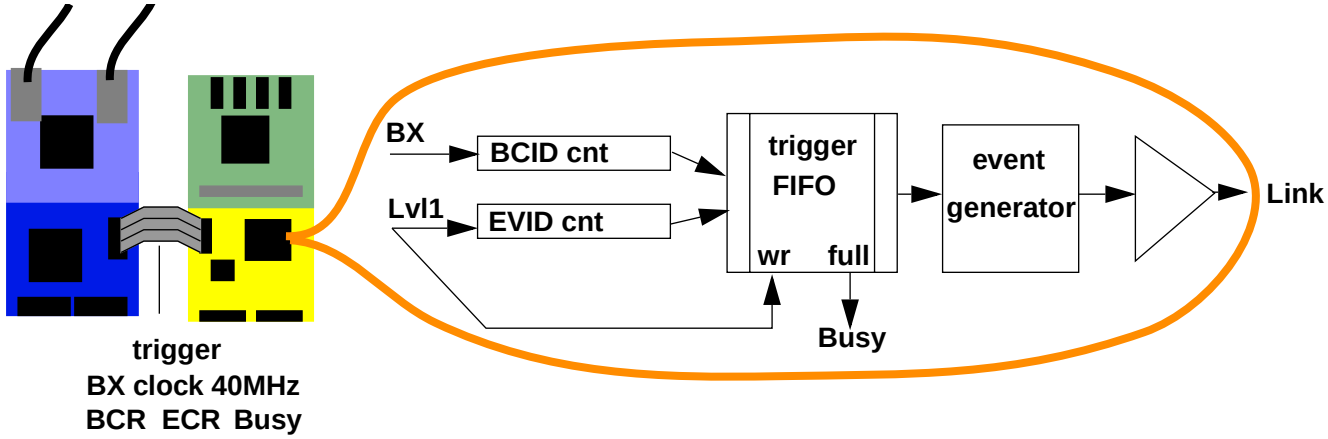


Interface to RUM defined

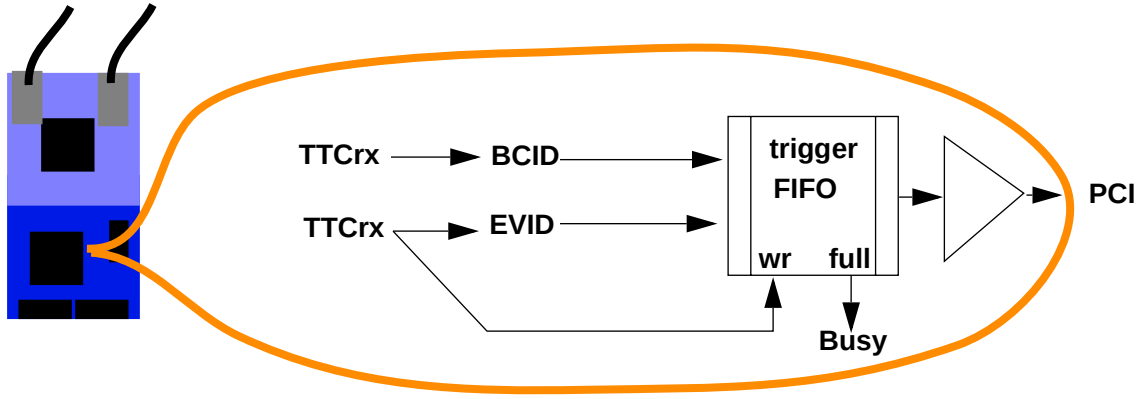
- Software RUM
  - RUM polls Descriptor Fifo
  - Reads out descriptor : event length, SDRAM startaddress
  - RUM initiates DMA from SDRAM to RUM via Gallileo
  - Interrupt indicates end of data transfer
  - RUM issues command to release memory in RUI
- Hardware RUM first possibility
  - Host computers acts as in case of Software RUM and issues in addition START and STOP command to RUM
- Hardware RUM second possibility
  - RUI issues start command to RUM (via one word DMA)
  - RUI initiates DMA transfer SDRAM -> RUM
  - Interrupt at End of DMA is caught by Host Computer
  - Host Computer issues END-command to RUM
  - Host Computer releases memory in RUI

Trigger receiver board

- At pseudo FED:



- In RM (PC, XDAQ):



Status

- Trigger TTCvx
  - Hardware exists and is working (Claudes setup)
- FED TTCrx
  - needs wires from TTCrx to Pseudo FED
  - easy to implement
- TTCrx at RM
  - exists (Claude modified his spy accordingly)
- Trigger generator (external logic, bricolage)
  - not yet present but simple
  - does not need computer access

Stage 2 : Software

- What do we need
  - This list in an elaborated form...
  - Control Software to setup the hardware blocks (Pseudo FED, RUI-DAQlink, RUM, RM)
  - Software for the RUM (software version)
  - Software to read out the RUM (software and hardware version)
  - Monitoring software to check data integrety
  - Performance measurement software
- Tools to use
  - XDAQ
  - I2O package to access hardware
- Status
  - Nothing exists so far
  - CS will write the software with help of “package experts” (Johannes, Luciano, Eric)

implementation of BUSY