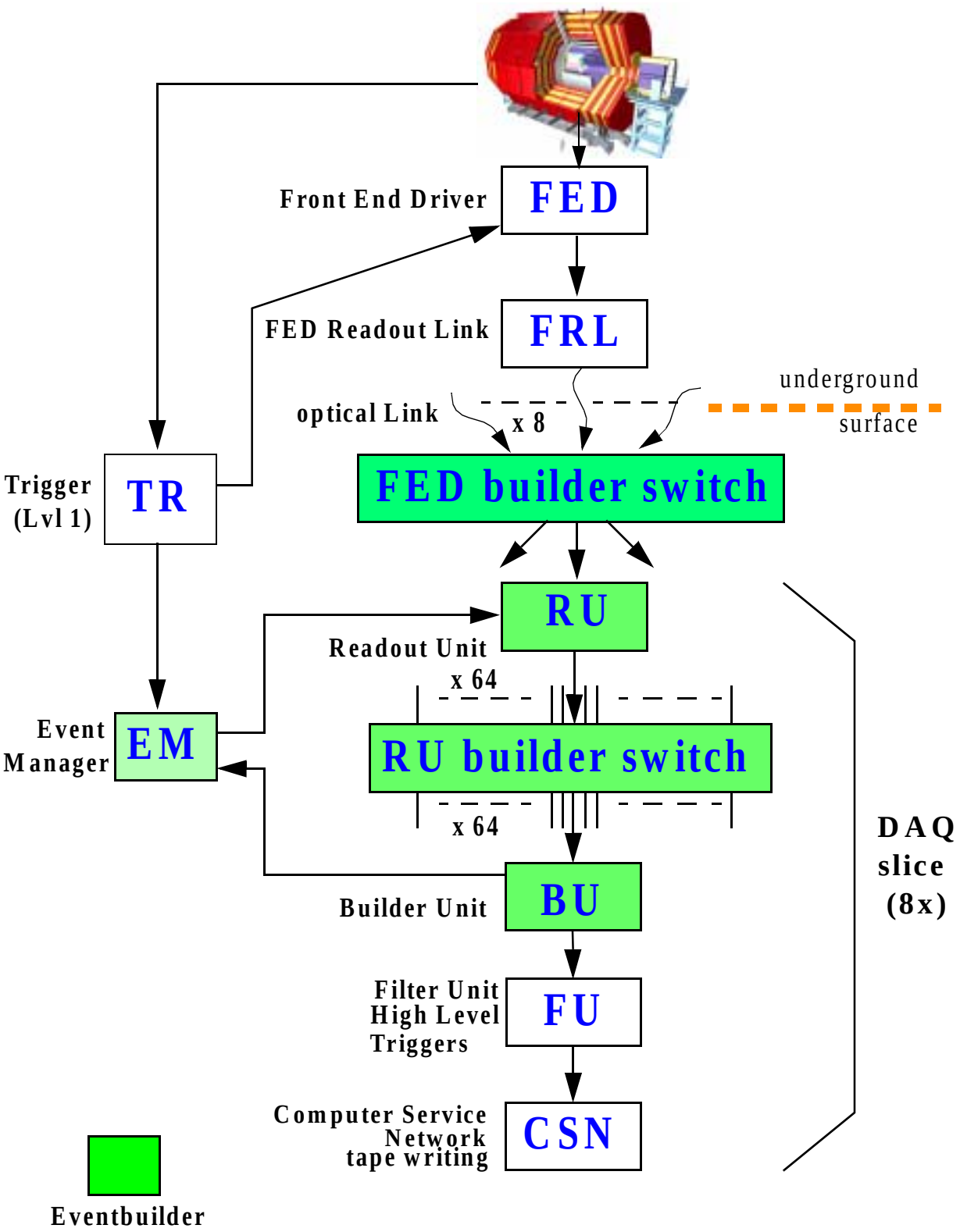
DAQ Column

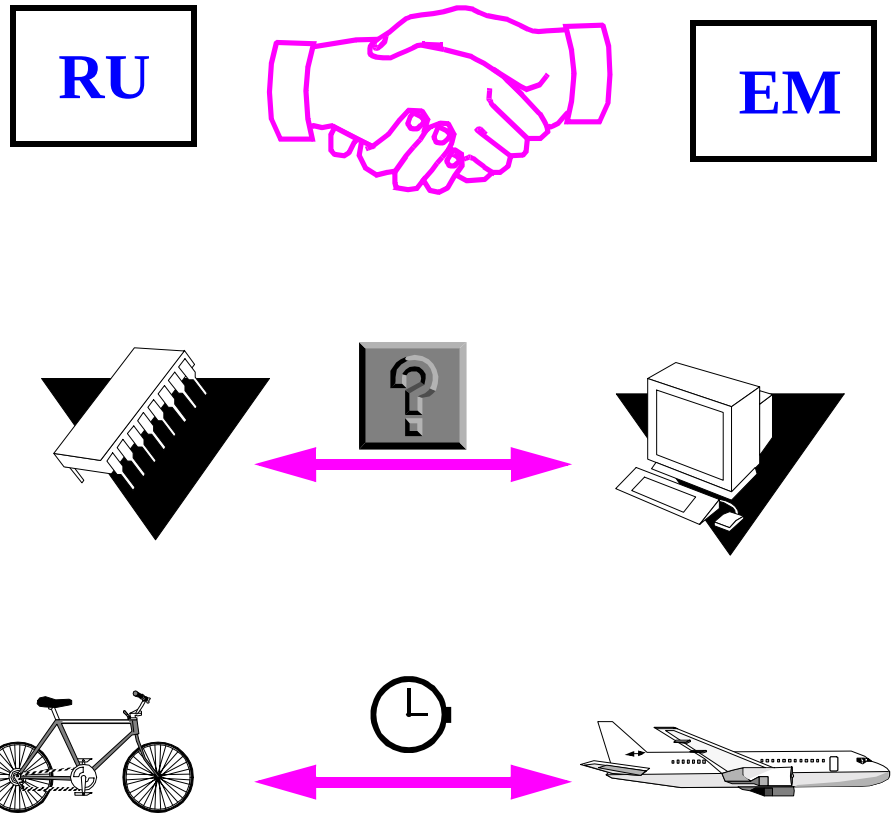
- Definition of the DAQ Column
- Purpose of the DAQ Column
- Status of the components
- Status of the integration
- To Do List

The CMS DAQ Columns

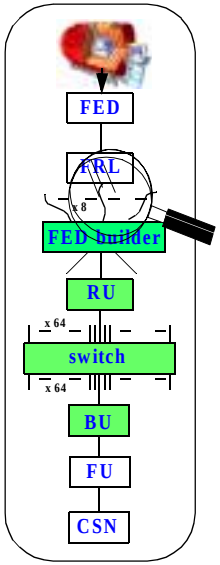


Purpose of the Column Prototype

- Need a test-bench to finalize R & D
  - Integrate FED prototypes
  - Develop Local DAQ system for FED
  - not included: EVB-switches
- Integrate hardware and software
  - test interfaces between different units
  - test protocols
- Try out different implementation options for final design
  - test bench for various technologies
  - find the border line between custom hardware <---> PC + software
- Measure performance
  - this is NOT the primary goal though

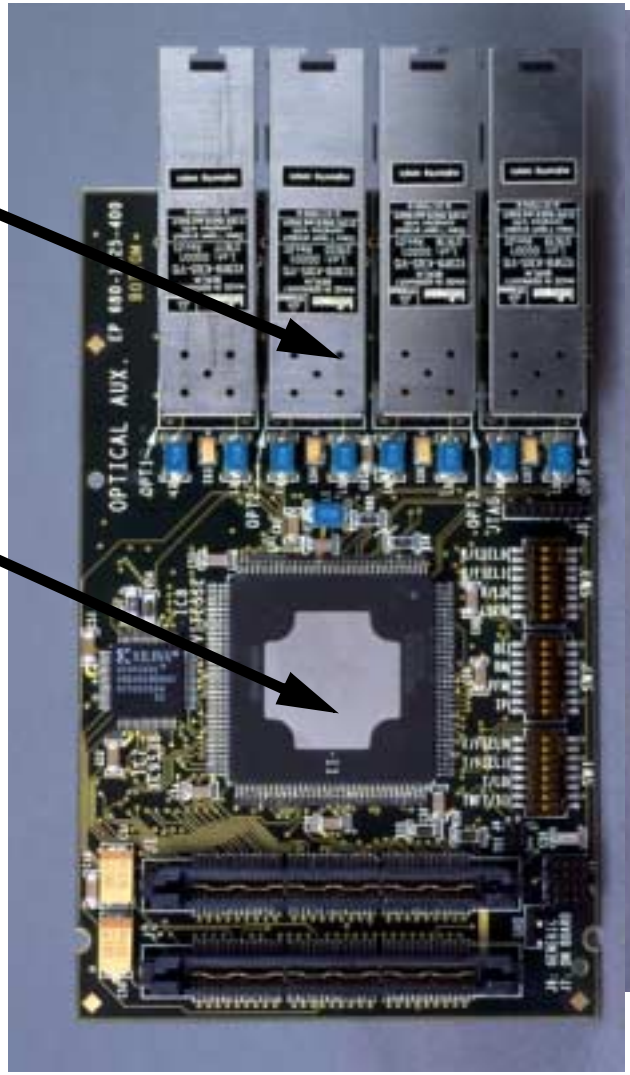


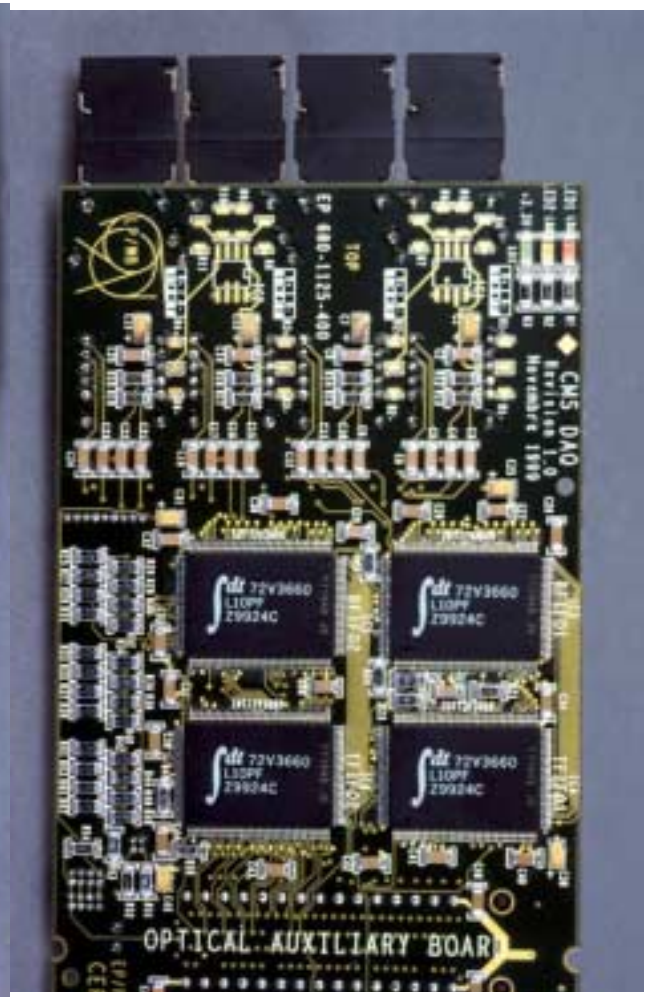
DAQ Column components : DAQ-Link



4 x Infineon
V23818-K305-V15

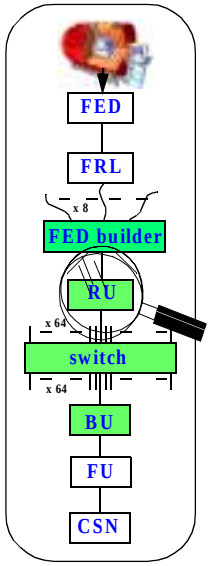
Vitesse
VSC7214





Readout Link :
full duplex
32bit / 100 MHz -> 400 MB / s
flow control implemented
prototype built and tested

Alternative : Commercial Link

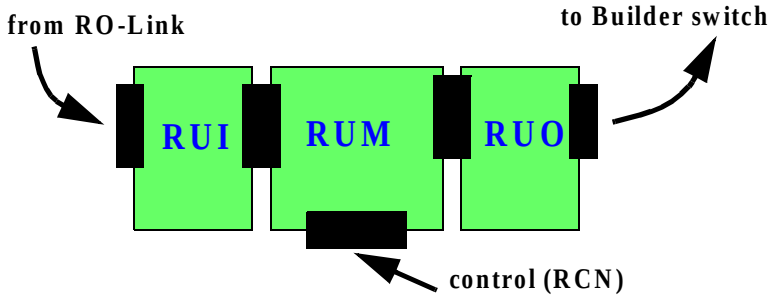


DAQ Column components : Readout Unit (RU)

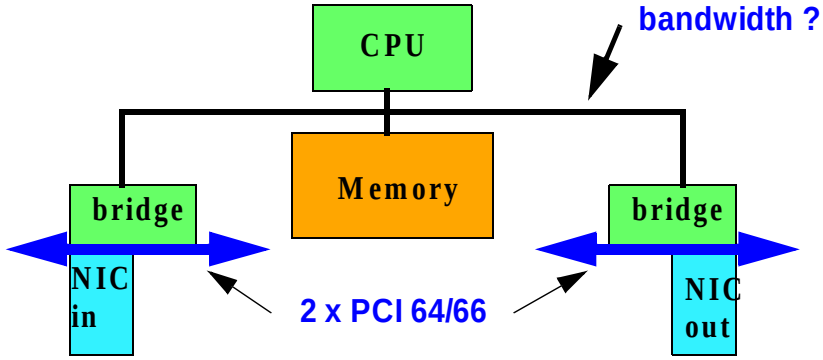
- Three logical components:
  - Readout Unit Input (RUI): Interface to FED Builder Network
  - Readout Unit Memory + Logic (RUM): buffers the data; sets up pointer tables to associate fragments with identifiers and destinations
  - Readout Unit Output (RUO): formats data for NIC card of RU builder

- Important question : custom hardware or PC + software

Hardware Implementation

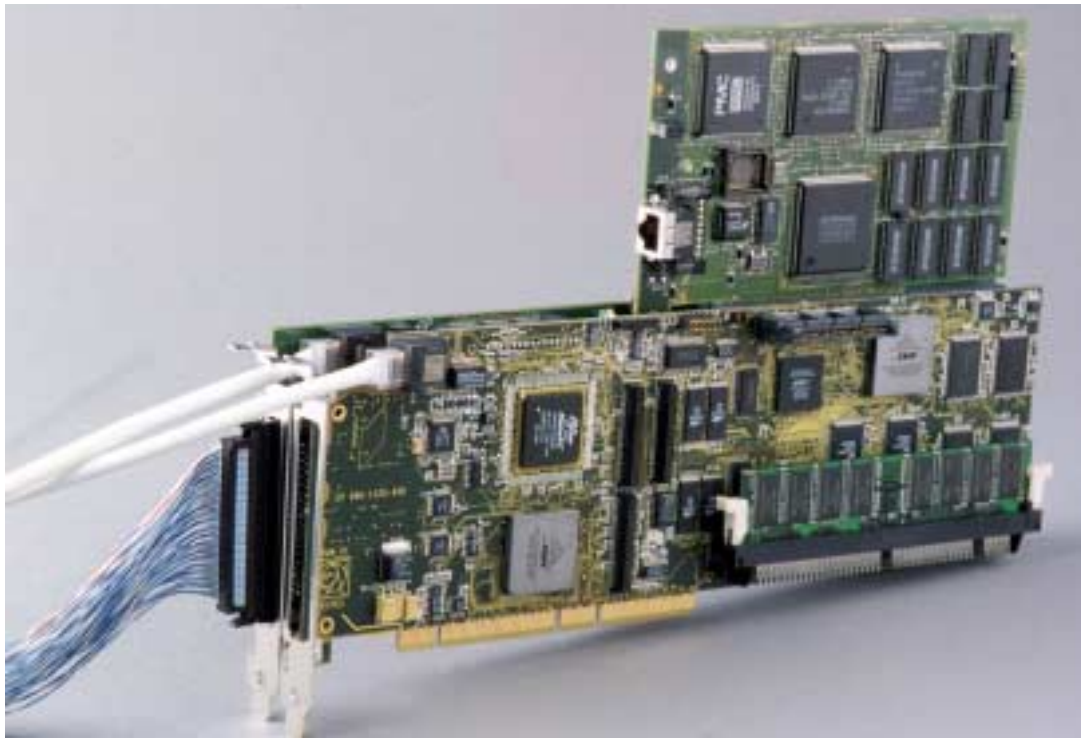


Software Implementation

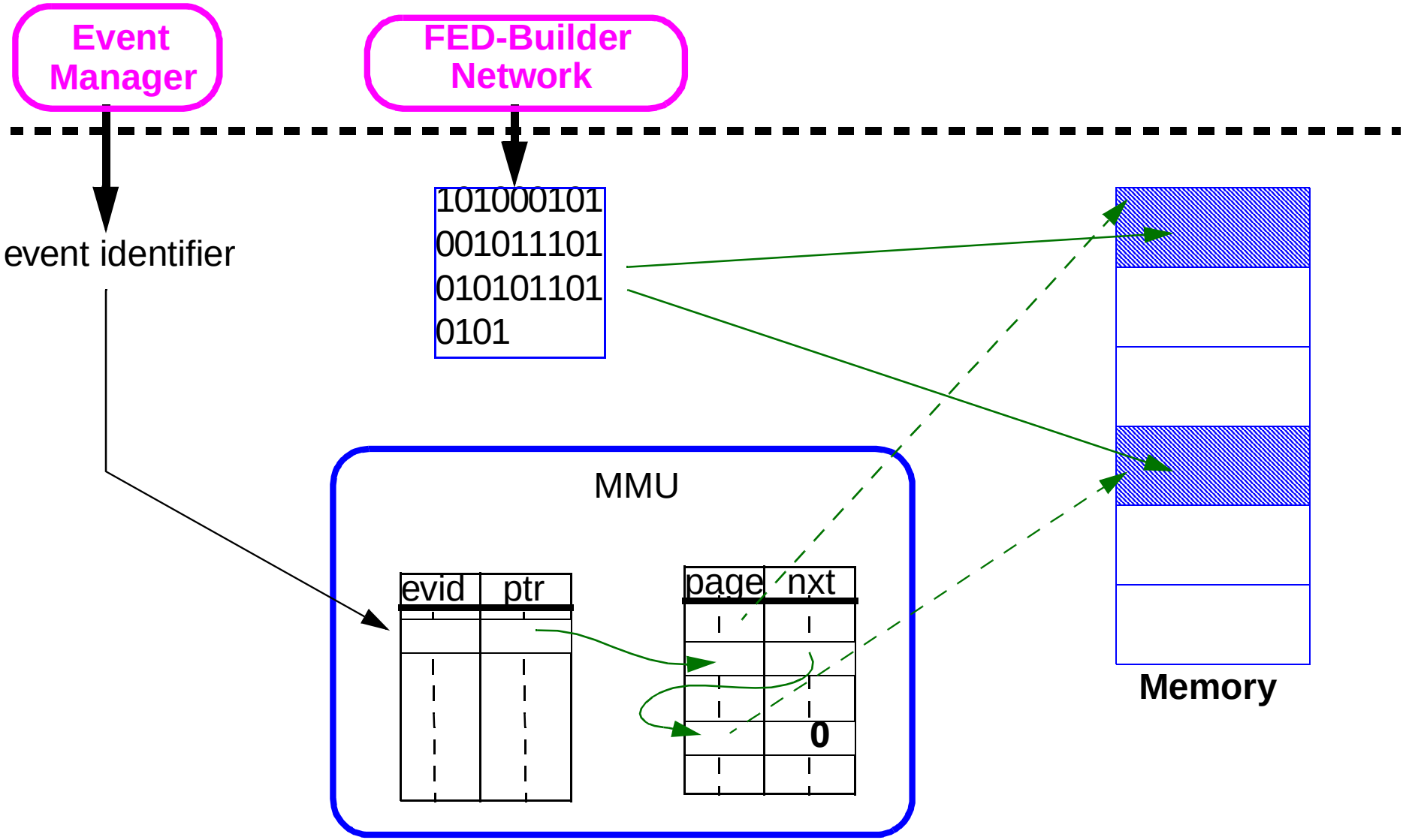


Hardware Implementation of RU

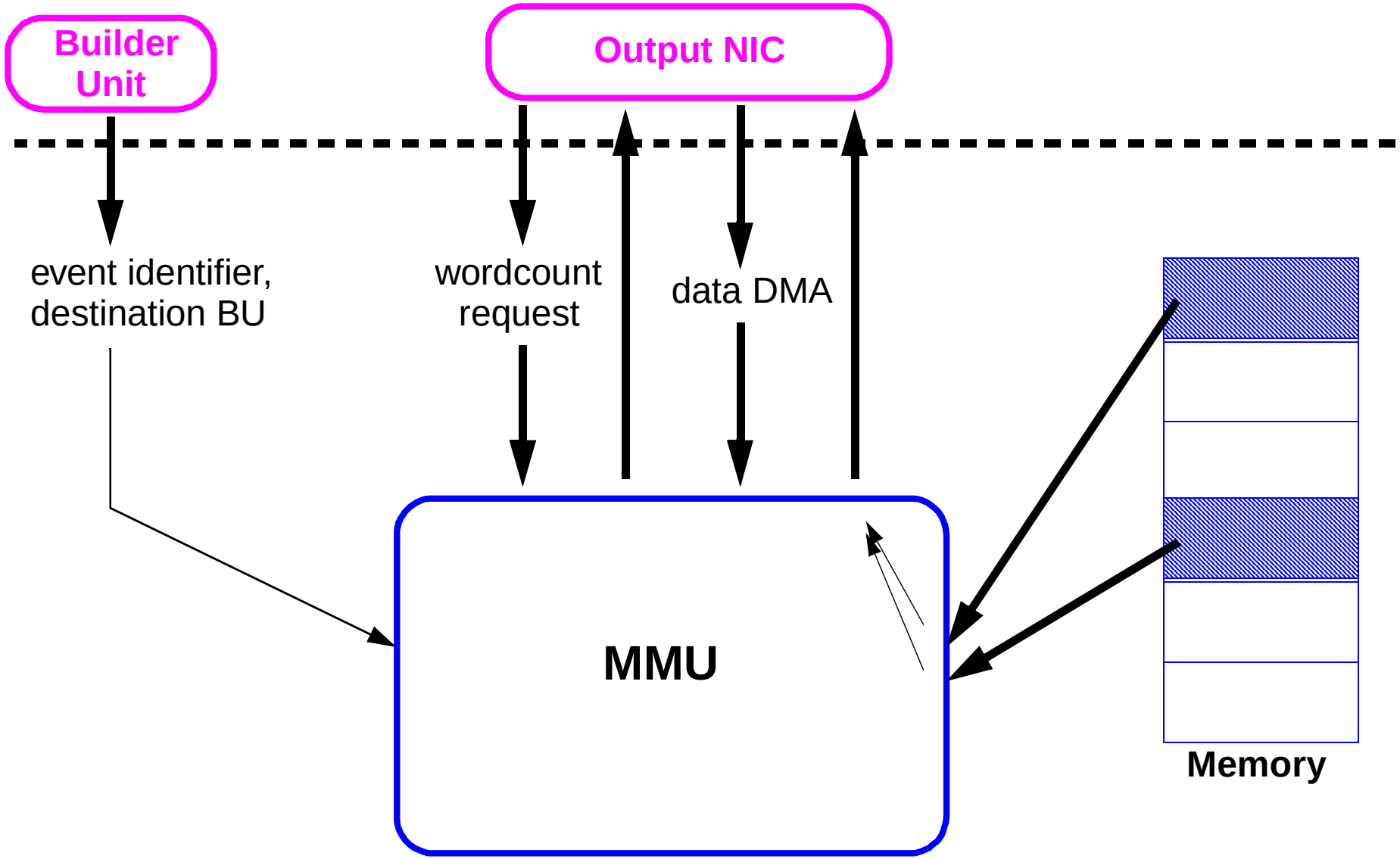
- Technical Features
  - Interfaces to outside world: 3 PCI buses (64 bit / 33 (66) MHz)
  - Implementation of all logic (including PCI interfaces) in FPGAs
  - 256MB of SDRAM
  - 1 MB of fast static RAM to contain tables of pointers



Hardware implementation of RU : Input functionality

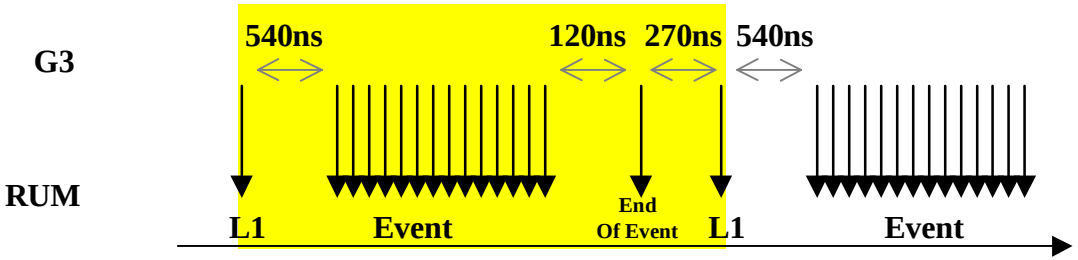


Hardware implementation of RU : Output functionality

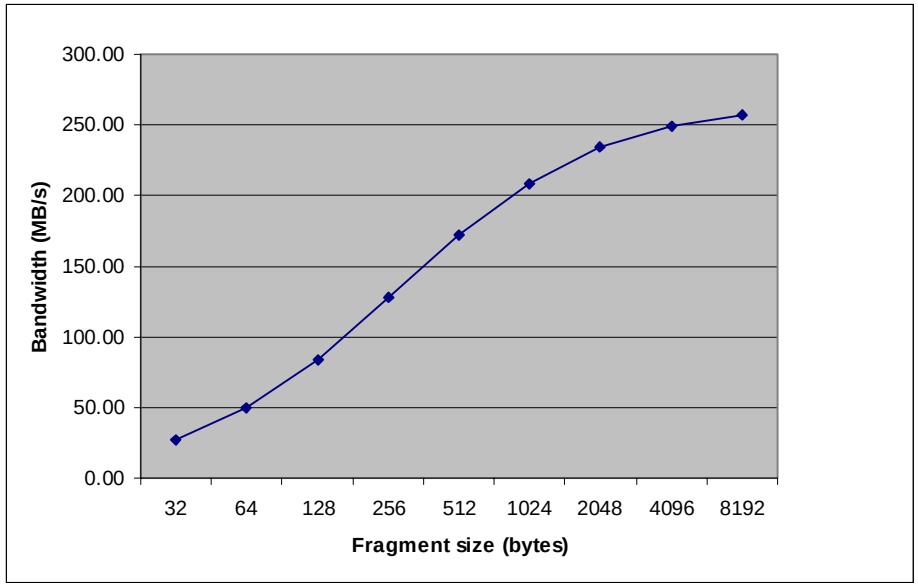


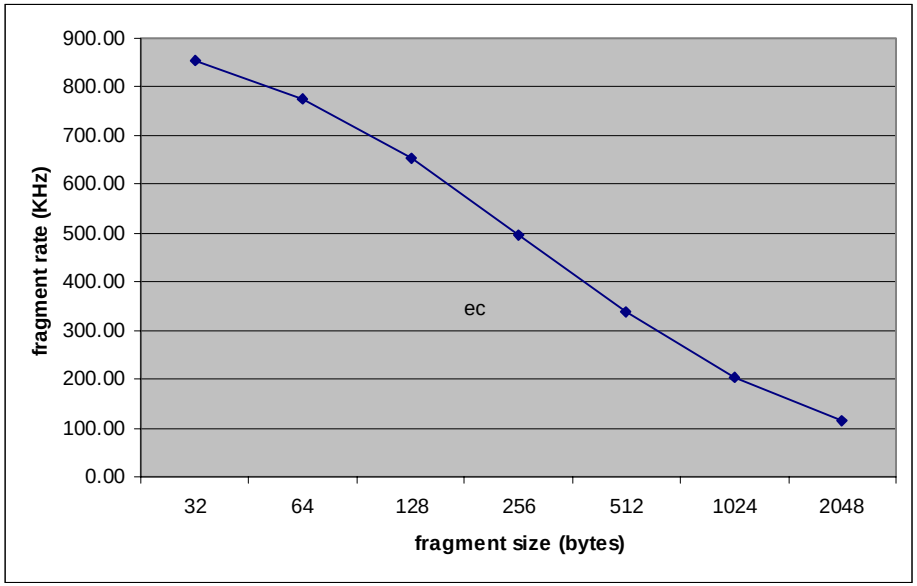
Hardware implementation RU : Results

- Input measurements:



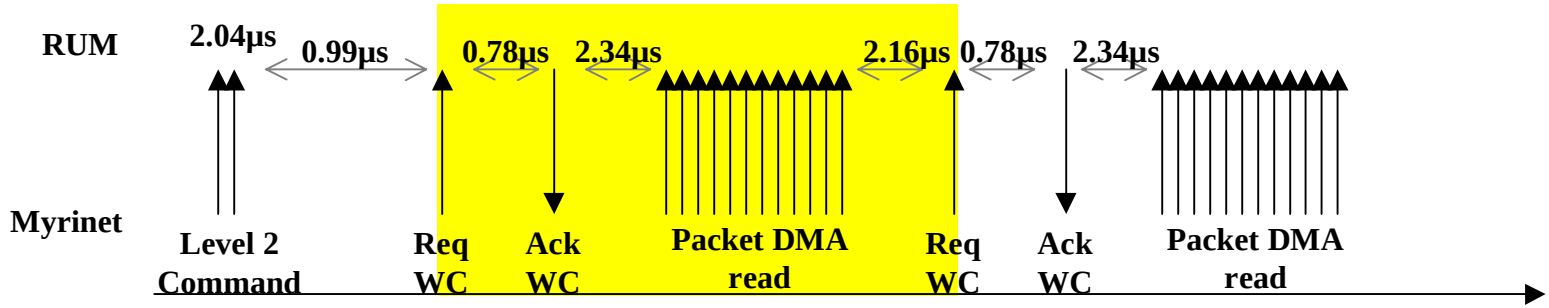
PCI 64 bit / 33 MHz



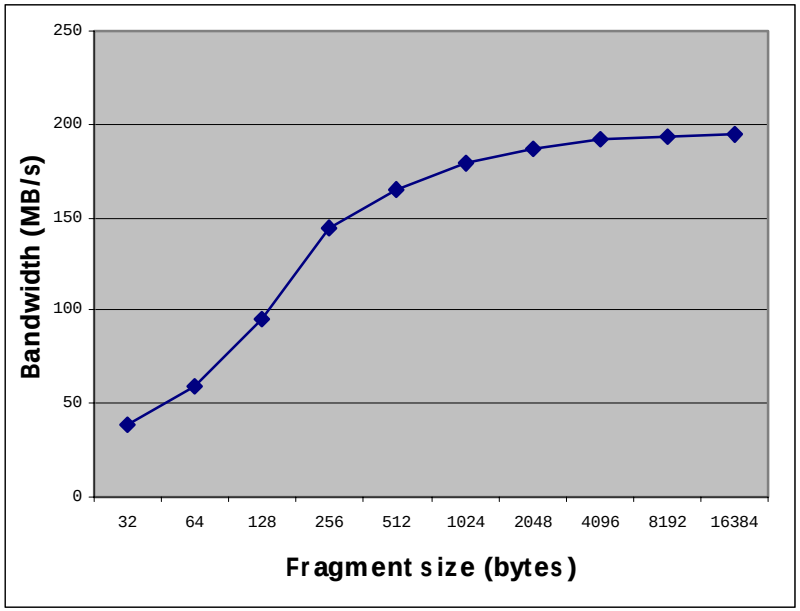


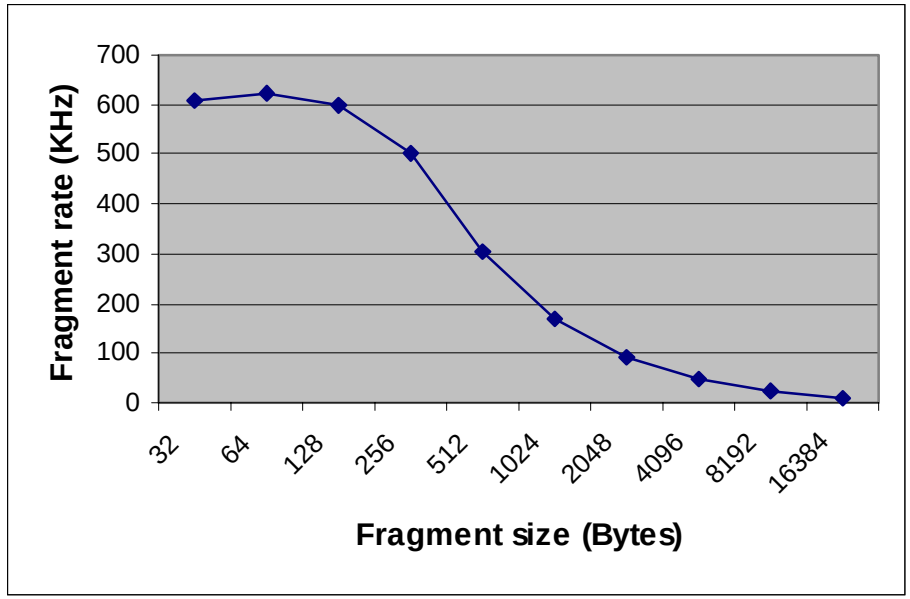
contd: hardware implementation RU: Results

- Output measurements



PCI 64 bit / 33 MHz



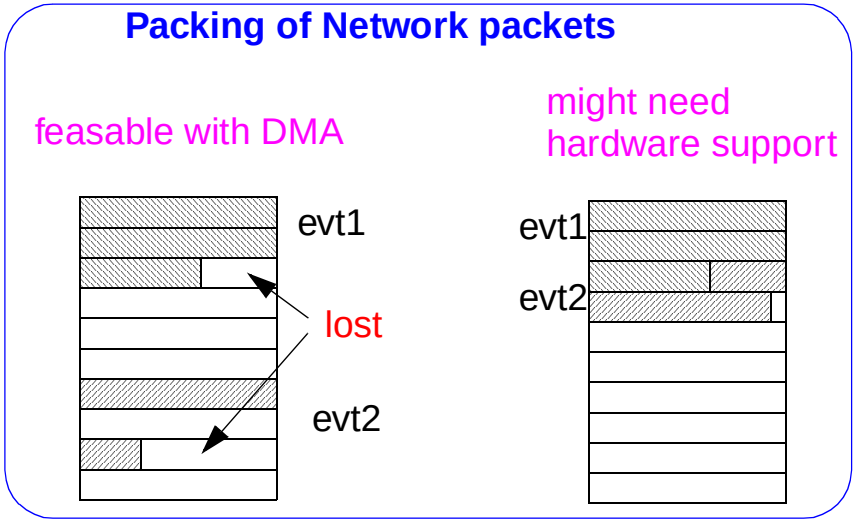


contd.: hardware implementation of RU : Results

- Measurements of input and output working together:
  (all with PCI 64 bit / 33 MB/sec!)
  - Myrinet NIC processor: 192 MB/s with 4 kB packet size (98 kHz)
  - Alteon Gigabit Ethernet NIC processor: 150MB/s with 4kB packet size
- **Conclusion:**
  - A hardware implementation of the RU has been successfully built and tested.
  - The required performance of 200 MB/s has been proven to be **achievable with to days standard electronic components**.
  - The current implementation needs intelligence in the output NIC card.
  - For the input some minimal intelligence is needed (DMA capability).
  - The measurements have to be compared to a software implementation of the RU.

Software implementation of RU : ongoing work

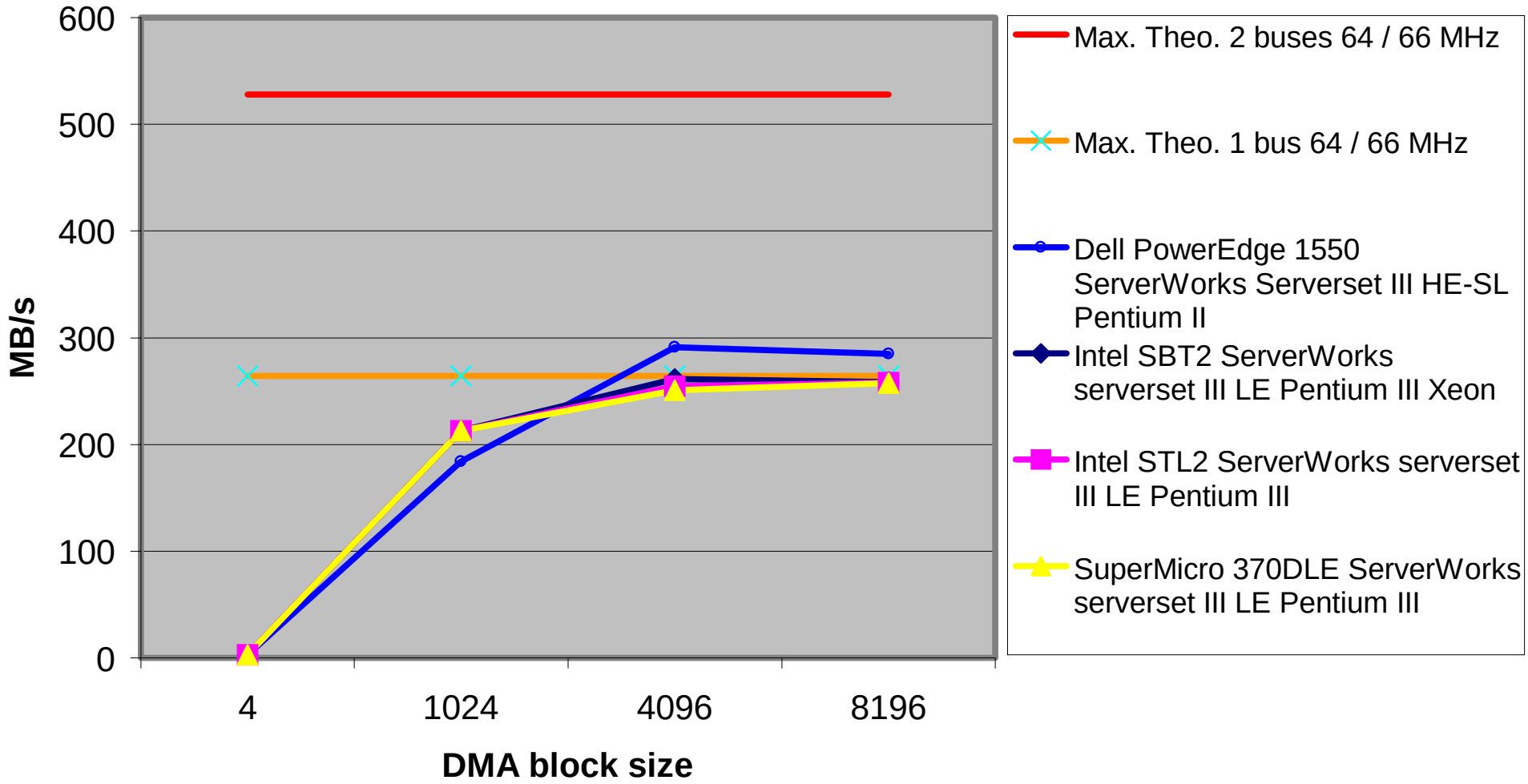
- Need for two independent PCI buses 64 bit / 66 MHz in order to sustain the data throughput rate of 200MB / s.
- Need for high memory bandwidth
  - Data is written to memory for buffering
  - Data is read from memory for transfer
  - The program resides in the memory
  - Perhaps data has to be copied during processing



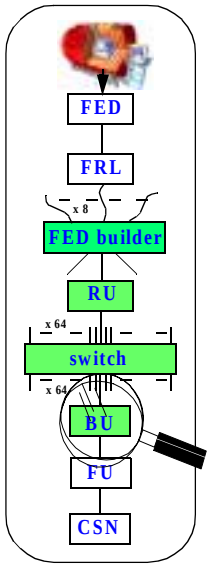
- Tests are starting with dual PCI bus (64 bit 66 MHz) server PC (Dell)

Software implementation of RU : first test results

64/66 simultaneous read and write



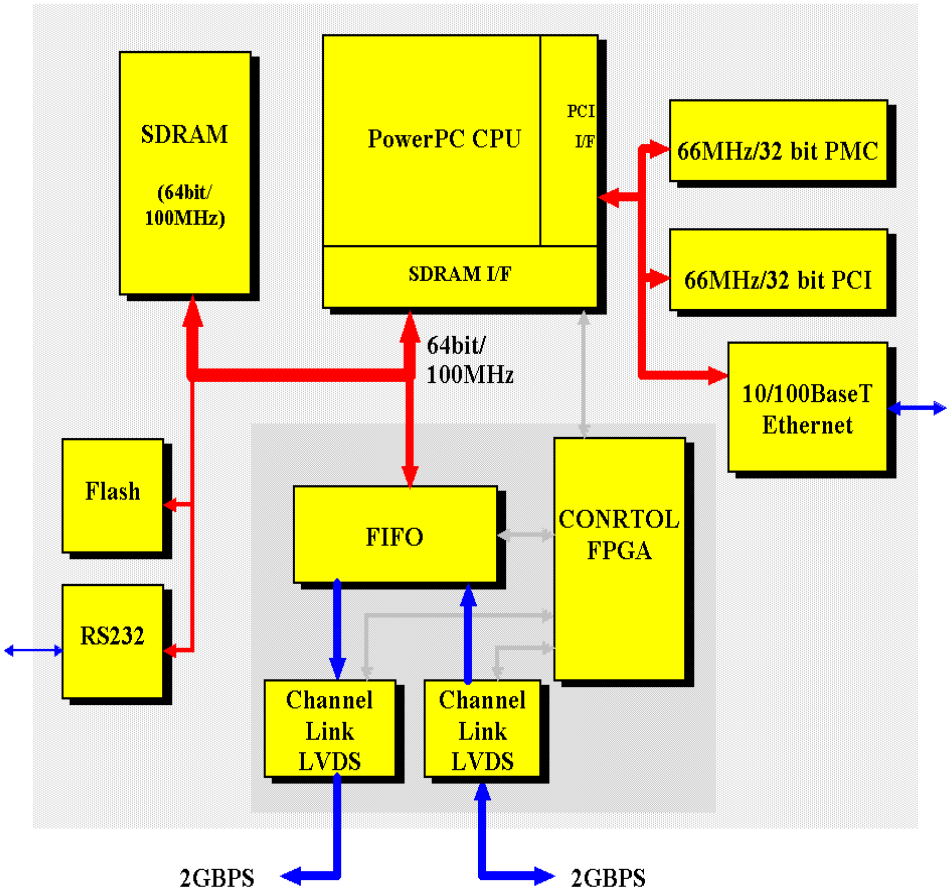
DAQ Column Components : the Builder Unit (BU)

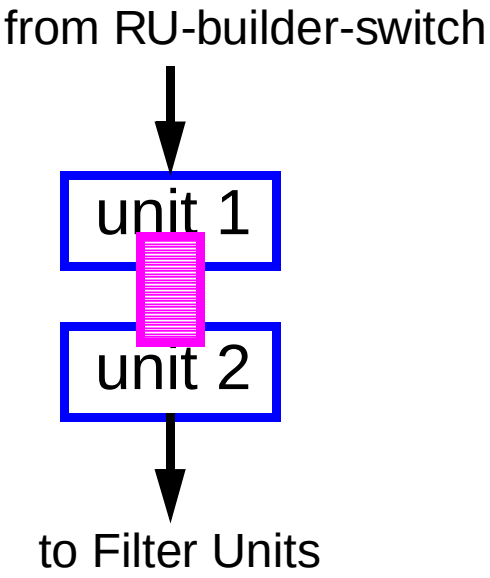


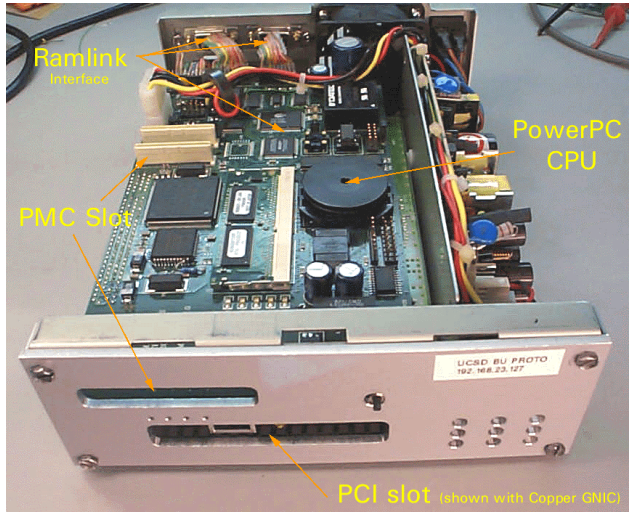
- Functionality
  - collect event fragments from RU-builder-switch and form entire events
  - transfer the events to filter units
- Possible solutions
  - similar functionality as RU -> similar options:
  - PC with high I/O capacity and high memory bandwidth or
  - custom hardware solution
- Hardware Prototype
  - has been built and debugged
  - Integration into DAQ system and measurements to be done

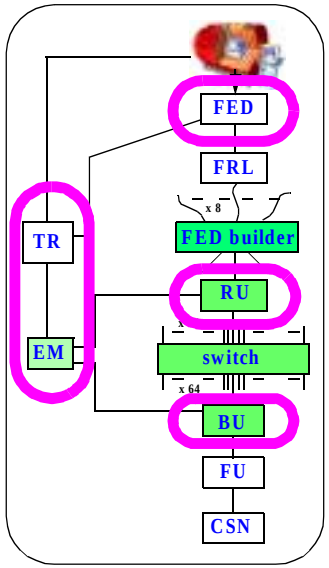
Builder Unit : hardware solution

Blockdiagram of hardware BU



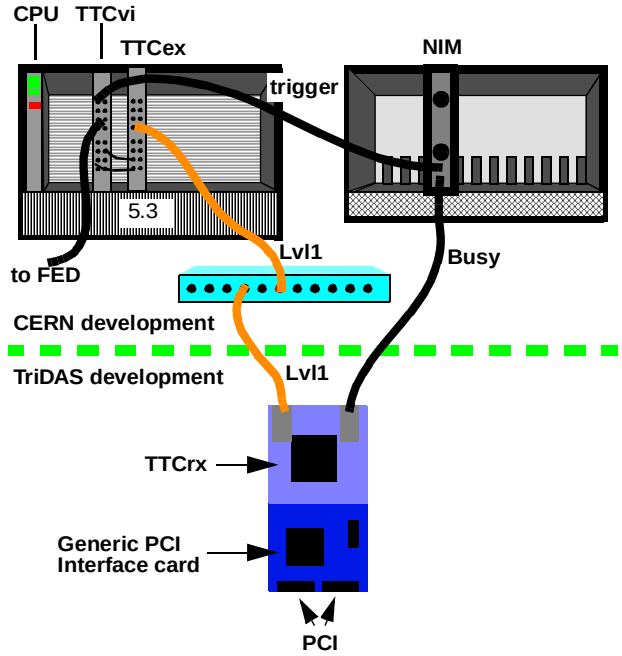




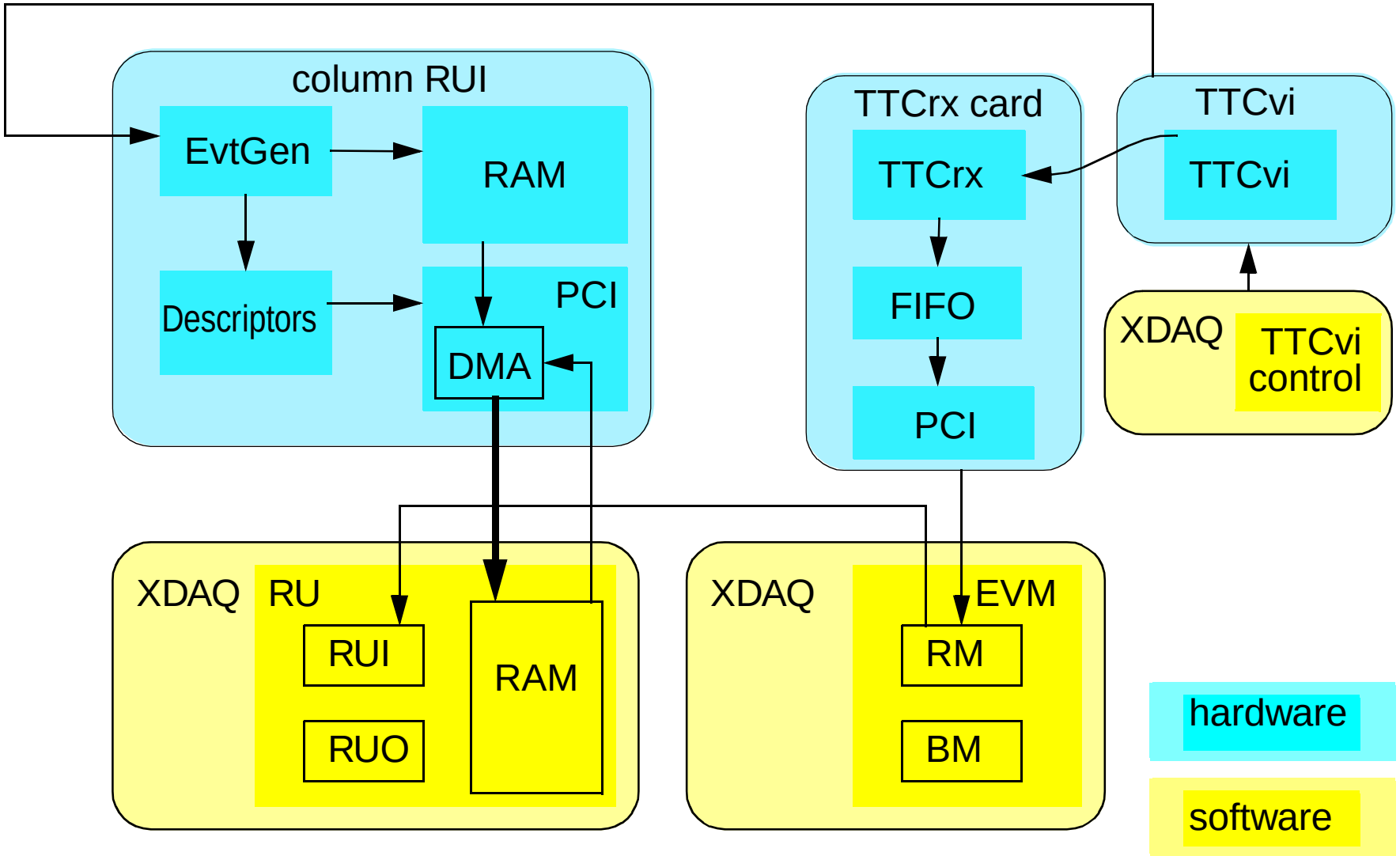


DAQ Column Integration : Putting it all together

- Components:
  - FED is implemented in a generic PCM card (Generic II : FPGA code)
  - no data Link yet
  - RU : hybrid software / hardware:
    - input stage is hardware (in Generic II: FPGA code)
    - RUM, RUO and BU are software (Motorola CPU (vxworks))
  - Trigger : NIM Logic with veto connected to TTC system
  - Event Manager: software interfaced to TTCrx setup
- Software
  - XDAQ framework for distributed DAQ system (see talk L.Orsini later)
  - application for each column-component in order to
    - start-up
    - control
    - perform DAQ tasks

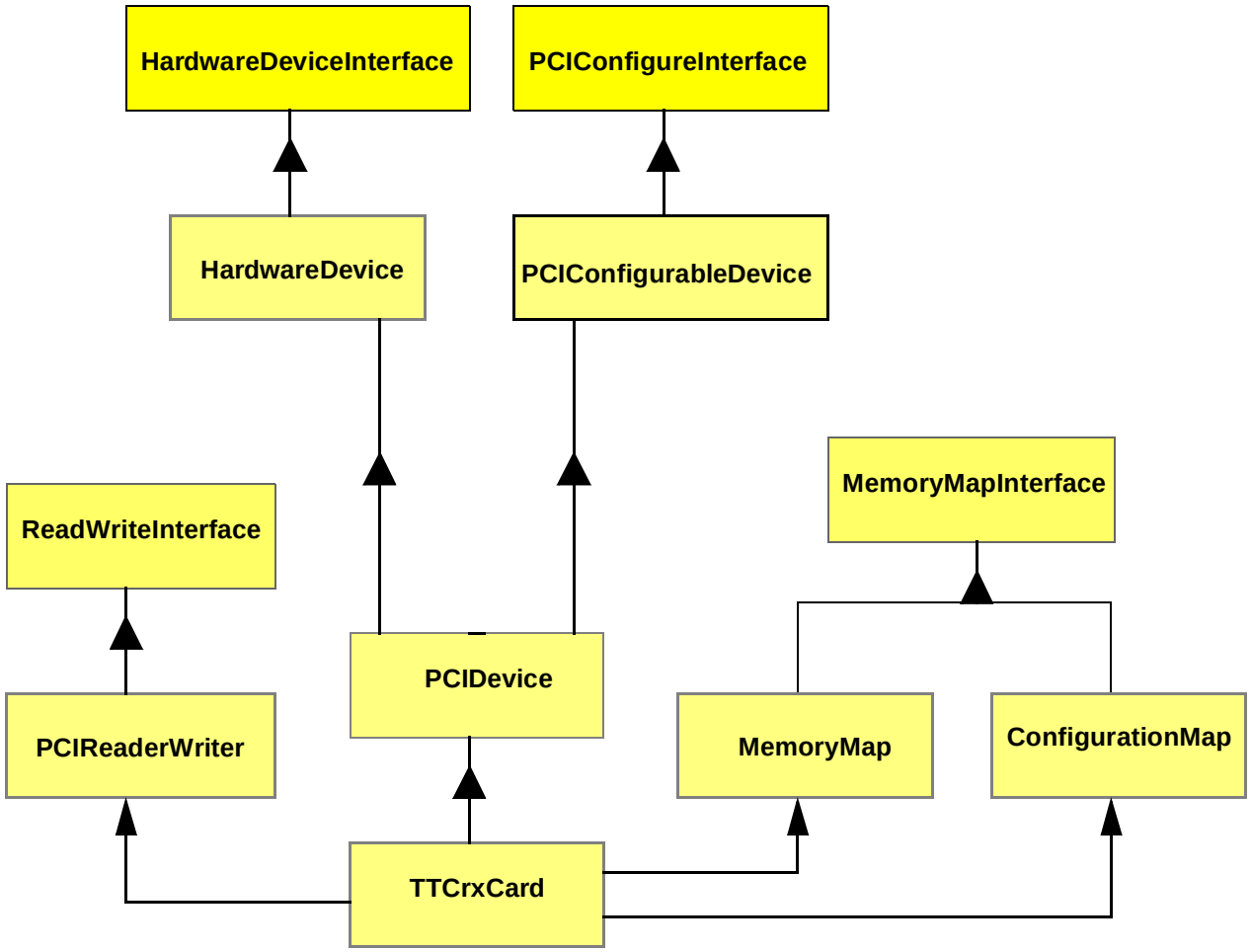


DAQ Column Integration: current setup



DAQ Column Integration : Hardware access library

- generic Hardware access library for PCI or VME cards
- platform specific libraries for Hardware Access
- hardware specific libraries with specific module functionality (for TTCvi, TTCrx)
- Design emphasis on “user friendly software”
- driven by human readable Memory Maps
- possibility of running scripts (for configuration, setup...)



Next Steps

- Evaluate DELL server with software implementation of RU
- Integrate a data Link into the column (Myrinet)
- Integrate Builder Unit after it has been evaluated
- Build and evaluate a software version of the BU on a powerful PC
- Design and build a FRL and integrate it in the column
- Integrate I2O core library (see next talk) and Hardware access library

DAQ Glossary used in this presentation

- FED (Front End Driver)
  - last element in subdetector dependent chain; Interface to DAQ System
  - formats data according in standard Frames
  - common hardware interface to DAQ System (Slink)
- Slink 64
  - physical and protocol definition of the interface FED - DAQ
  - protocol like a “write” operation to a hardware FIFO
  - 64 bits data width
  - up to 100 MHz clock frequency (not necessarily used in CMS)
- FRL (Front End Readout Link)
  - LVDS link which transfers data from FED Slink port to a receiver card housed in PC.
  - Receiver allows to merge data of several FEDs (max. 3)
  - FRL needs to house Interface to DAQ - Link (see different options discussed in talk of A.R.)

- DAQ Link
  - transfers data from underground to surface (O(150m)).
  - require 400MB/s and flow control
  - Interface to FED builder
  - commercial candidates on the market (Myrinet, Gigabit Ethernet ...)
- FED builder
  - performs event building for eight FEDs.
  - 1 - 8 outputs connected to 1 - 8 DAQ slices
  - system is scalable from this stage on (a minimal system needs one slice only)
- EVM (Event Manager)
  - Interface of DAQ System to Trigger
  - implements the Event Builder Protocol, involving the RUs and the BUs (see below)
  - manages the event-identifiers

The following items define a DAQ slice:

- RU (Readout Unit)
  - receives : - data - fragments of the FED Builder (approx. 12 kB)
    - for each Lvl1 Trigger a Trigger Identifier from the Event Manager
    - readout requests from the Builder Unit
  - tasks : - the RU contains the buffer memory of the DAQ system
    - associates event fragments with unique identifiers needed for event building
    - perform event building with the RU-builder protocol.
- RU builder
  - switch to perform event-building
  - 64 inputs and 64 outputs
- BU (Builder Unit)
  - sends requests for an event identifier to EVM
  - requests event fragments for that identifier from RUs
  - builds entire events
  - forwards events to Filter units

- FU (Filter Unit)
  - performs level two trigger decision by processing data of entire event.
  - monitors data quality online
- CSN (Computer Service Network)
  - forwards events accepted by Lvl2 to computing services at CERN for mass storage