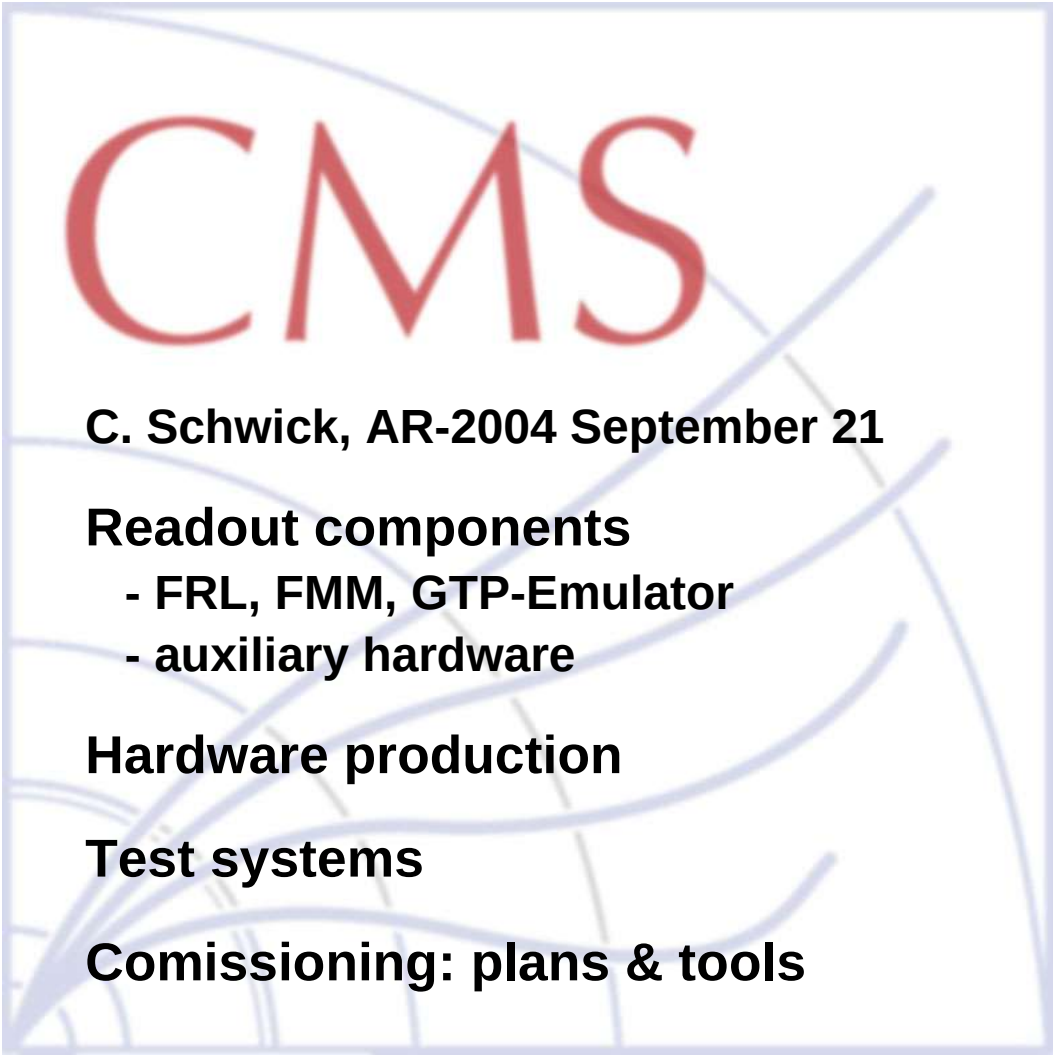
# DAQ annual review 2003

# Final design: Prototypes




C. Schwick, AR-2004 September 21

**Readout components**
- FRL, FMM, GTP-Emulator
- auxiliary hardware

**Hardware production**

**Test systems**

**Comissioning: plans & tools**

http://cmsdoc.cern.ch/cms/TRIDAS/html/Referee.html

# Introduction

- Status of last review:
  - Main Hardware components
    - SLINK64 : ready for production
    - FRL : function prototype
    - FMM first prototype
    - GTP emulator : first prototype (at Athens)
    - Trigger distributor: under development
    - sTTS aTTS interface: to be designed
  - Auxiliary Hardware components
    - FED emulator : available
    - FMM extender : planned

# contd Intro

- Hardware modules integration status of last review
  - SLINK : FIRST prototype in TDRDemonstrator
  - FRL: implemented by emulator (GIII)
  - FMM : not integrated (NIM  logic for backpressure)
  - GTP emulator: not integrated (GIII mockup)

# contd intro

- LVDS Cables status of last year:
  - Test on 3 lengths of 3M (5m 10m 15m)
  - No statistical tests
  - No different vendors

# FRL final design

- FRL preseries design (bring module with SLINK)
  - Slight change in PCI interface (firmware) in order to work around a problem in PC-BIOS
    - this problem prevented to pack a crate with 16 FRLs since memory space is wasted by the allocation scheme in the BIOS
    - Now an FRL with the Myrinet card is seen from the PCI bus like three independent PCI cards. No PCI bridge in FRL module.
- Changes for final series production
  - evaluating a small layout change for LVDS receivers side termination

# Contd.: FRL

- New: Add on merger card in order to merge up to 4 FEDs into one FRL
  - test bench for improved termination scheme of LVDS signals:
    - new  design terminates also high frequency common mode signals
    - reduces high frequency noise in cable shielding
    - less noise radiated into environment
    - protection against common mode reflections/resonances in cable

# LVDS cables

- Test setup which determines the maximal frequency until first BERR in n seconds
- produce tests with new add on card (new termination scheme) to be done
- compare Amphenol with 3M on that setup
  - generate plots
  - show eyes

- cite BERR rates measured so far
- Find arguments why we go for 3M

# Trigger Distributor

- Final protoype is existing
  - Serves as multi purpose module
    - Trigger distribution in FRL test mode
    - Backpressure collector in FRL test mode
    - Crate power controller in test system
    - Crate monitoring for expert debugging:
      - Trigger distributor contains Ethernet interface with Web Server.
      - Software for this is currently under development (summer student)

# TTS-FMM-FMM Extender

- Under development: FMM final prototype
  - New form factor Compact PCI
  - New number of inputs / outputs
  - Contains “reused” Compact PCI interface
  - Contains larger FPGA in order to implement deadtime monitoring
- Under development: FMM extender
  - Diagram with inputs and outputs
  - Usage:
    - test the FMM module
    - In Preseries:
      - Collect PseudoFED backpressure signals and convert them to FMM signals which then are Fed into FMM
  - Status: protoypes exist, problem with component soldering

- To be done (hardware)
  - Hardware interface to TTS system for aTTS server

# Production / Testing

- Experience of Preseries:
  - 70 FRLs fully mounted and tested
  - no major problems with PCB or soldering companies.
    - some smaller (=repairable) problems with component soldering

- Testing
  - Three stages are foreseen
    - Stage one bank
      - Optical inspection
      - Electrical inpection (current consumption)
      - Firmware downloading
      - insertion into database
    - Stage two
      - Testing of all electrical connections of the board including input and output
      - Software driven
      - Test software under development

# contd Production/Testing

- Stage 3
  - Long term tests
  - will be used to test the LVDS cables and long term (many hours) data transfer through the FRL
  - design is close to stage 2

# Production

- Series production
  - PCB “price inquiry” has gone through CERN Finance division
    - Offers have been received
    - Probably the company we wanted will win the contract
  - Component “price inquiry” is on the way
  - Component soldering “price inquiry” is on the way
  - Cable “price inquiry” in preparation

# Comissioning

- When components will be inserted in CMS they will have passed the tests on the described test benches
- Test to be carried out in place in the final system:
  - SLINK64 self test (needs only power from FED)
  - FRL generates data and feeds them into the system (FRL self test mode)
    - operates with GTP emulator
    - triggers will be distributed via trigger distributor
    - FMM signals will be generated by FRLs and trigger distributors
    - dedicated FMM will collect the 32 FMM signals from FRL crates and feed them back to trigger emulator
  - FRL self test mode with “Real data” read in from file.
    - FRL will cycle through a limited amount of event fragments stored in SDRAM

# Comissioning

- Data taking comissioning:
  - Local FRL DAQ allows to read out the whole CMS detector at the level of the FRL.
    - Over Gigabit Ethernet the data can be sent from the FRL controller PC to Event Builder applications ( BU if RU is housed in FRL Controller PC)
    - allows data taking at low rate without FED-Builder and/or RU-Builder running.
  - Spying during data taking at the FRL allows to check for data consistency or debugging at the FRL level without disturbing the main data acquisition activity.
  - The FRL can produce simple histograms taking into accout every event (word count histograms)