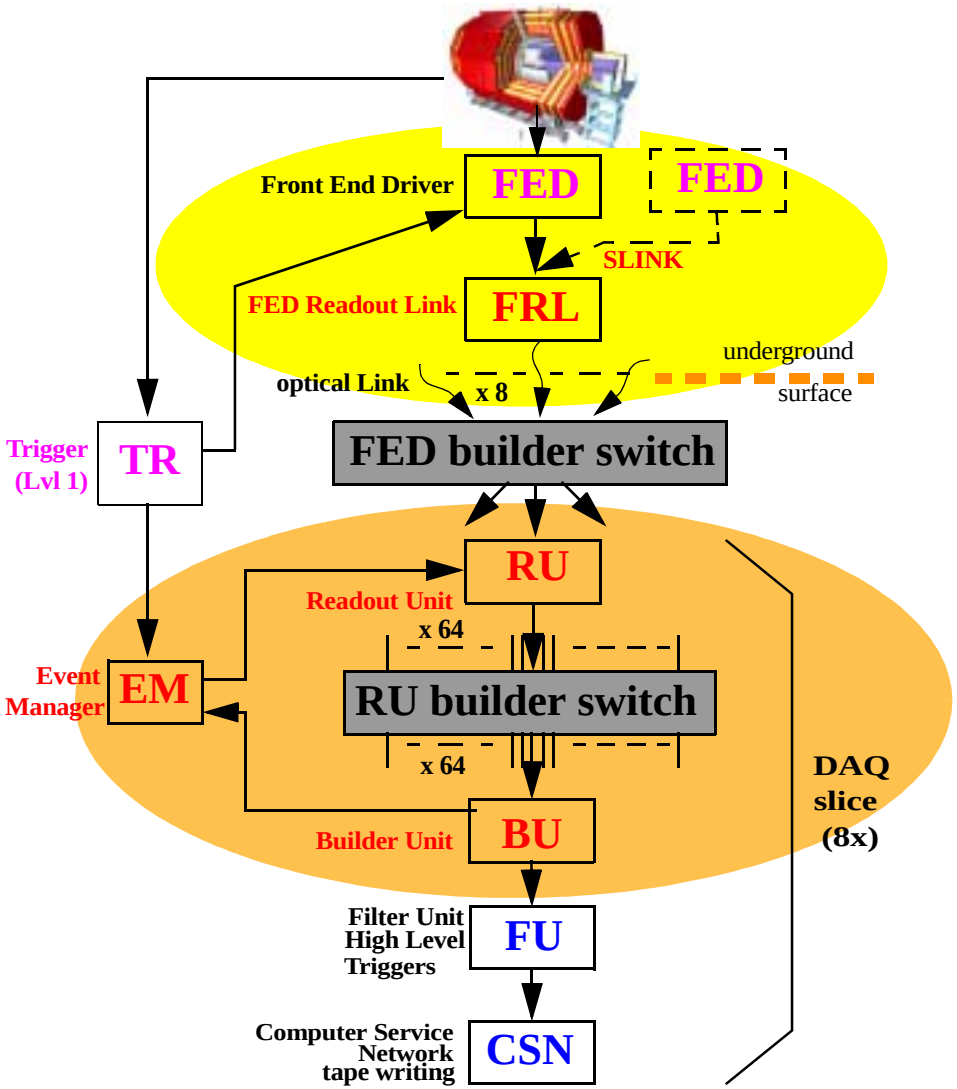
DAQ Column Status

- Architeture
- Lessons learned
- Summary

DAQ column components

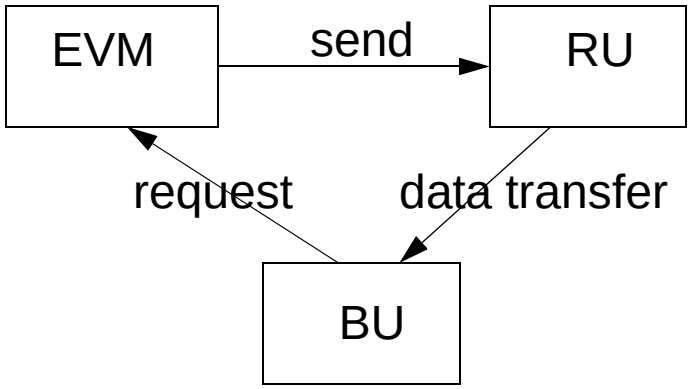
- Components of Column
- needed but not a component of Column
- EVB components
- Column components (not currently considered)

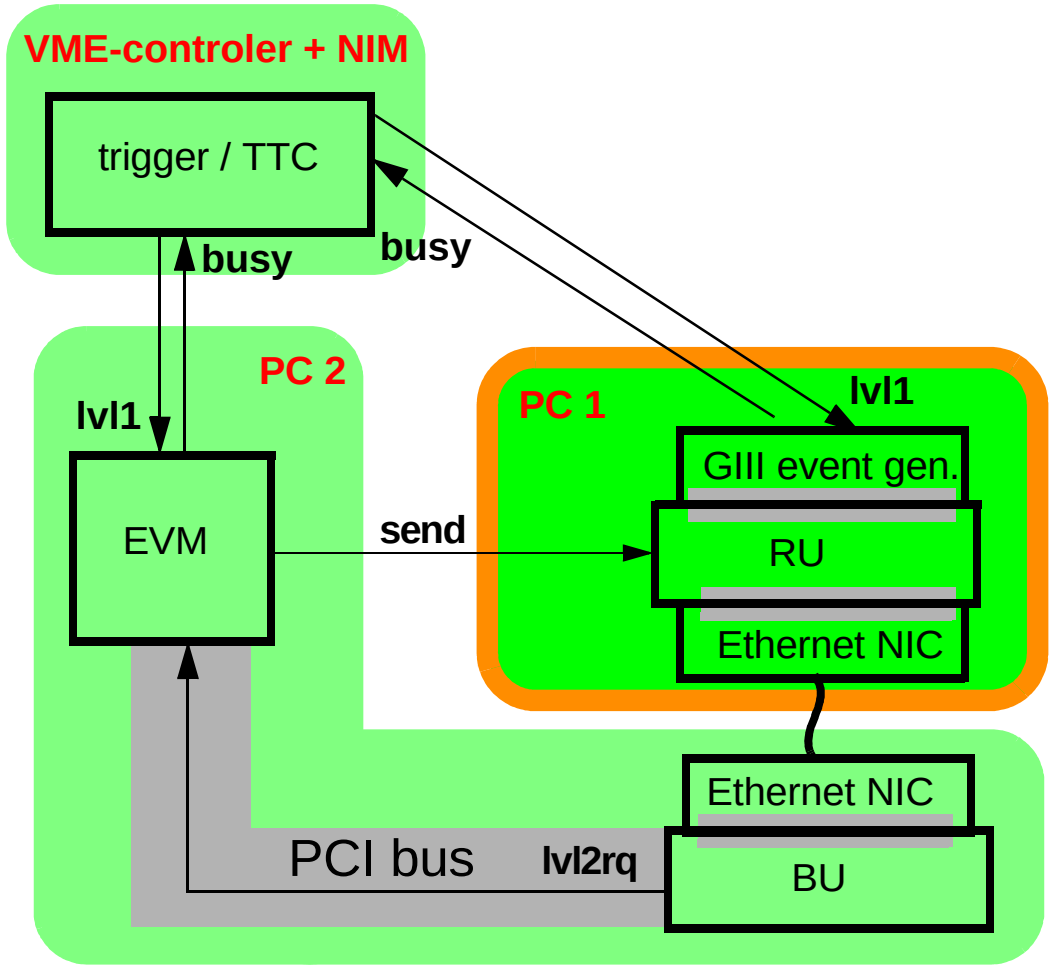
- Currently: 2 Activities
  - FRL region tests SLINK, Merger, FRL
  - RU / BU region: build platform for PC tests



Current Architecture

- Components:
  - EVM: TTC system with new TTCrx readout system.
  - Data source: modified Fedkit with trigger input and busy output. Event sizes according to programmable table.
- Protocol (indirect mode):





Architectural variations:

- All set ups so far with Ethernet 100Mb connections
- The same components have been housed in different combinations on hosts:

PC 1	PC 2	PC 3	rate [kHz]	remark
FLT	EVM, RU	BU	5.5	network limited
FLT, BU	EVM, RU	-	5.5	network limited
FLT, BU, EVM	RU	-	5.4	network limited
FLT	EVM,RU,BU	-	15.5	TTCrx readout limited

- Not yet stable

Lessons learned so far

- The tests have revealed problems on all levels of the system:
  - XDAQ application bugs (DAQColumn software)
  - problems/features in XDAQ
  - problems in the Fedkit software
  - problems in the Fedkit hardware
- XDAQ / XDAQ application lessons
  - Complicated multiple-inheritance structures: User must have a good knowledge of the typical inheritance trees and the composition of a typical XDAQ application. Need to study well the examples and manuals and sometime source-code.
  - somtimes “insider knowledge” still necessary.
    example: knowledge about mechanism how the send of i2o frames:
    a) within one xdaq executable (involves software fifos based on lists which might overflow since they do not block)
    b) between different hosts (peer to peer transport over network)

- Fedkit (hardware & software) lessons
  - initalization of a suspend flag had been missing — fixed
  - problem in block alignment with reserved header-space — fixed
  - Incompatibility of Block chains and memory allocation between XDAQ and fedkit — fixed
  - PCI access problem under very specific cirumstances (retry due to congestion on PCI bus at end of event) — fixed
- Currently one unsolved problem
  - Event fragment is returned from fedkit BEFORE the relevant DMA — unfixed

Summary

- Some of the problems have been found after successfull transfer of several hundreds of millions of fragments.
- Problems show up under very specific situations
  - some problems occurred at NON-maximal performance (in some trigger rate range)
  - need “congestions” on PCI bus in special situation to provoke error
- Behaviour depends on grouping of components
  - what application runs on what computer
  - message passing between applications is different if running in the same XDAQ executable
- Next steps
  - first priority: get a stable system running
  - use GM for RU-BU data transport (work has started by Akos)
  - measure data throughput (once system is stable