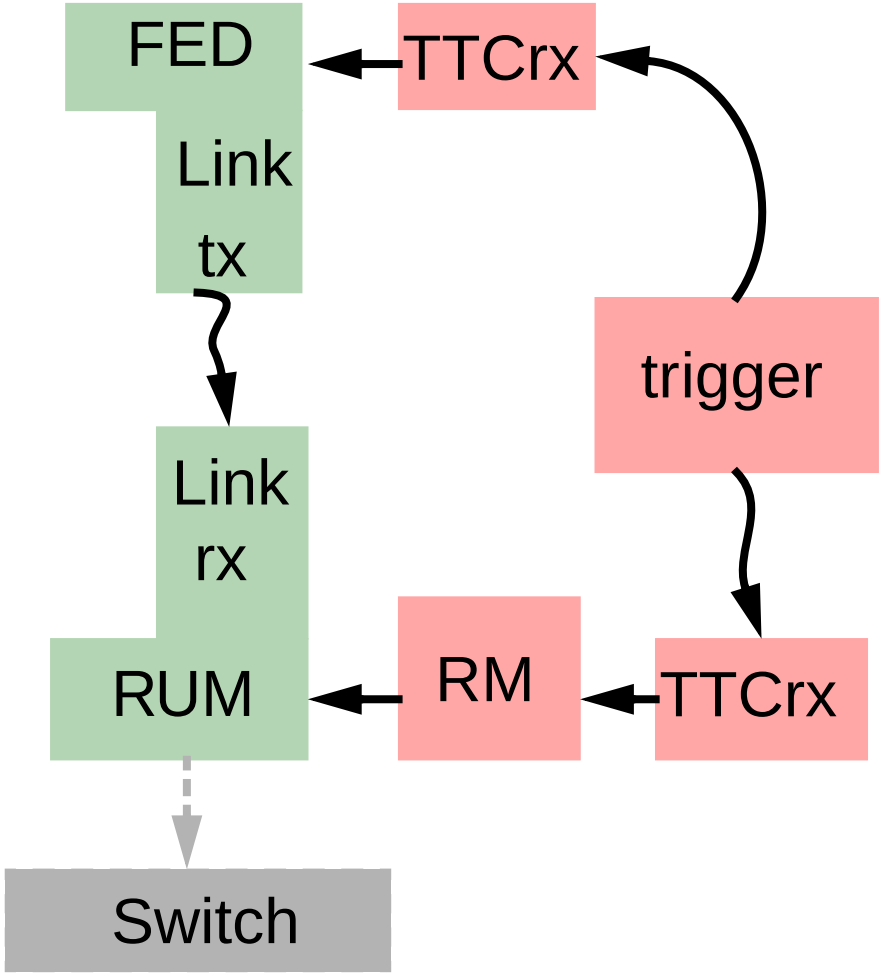
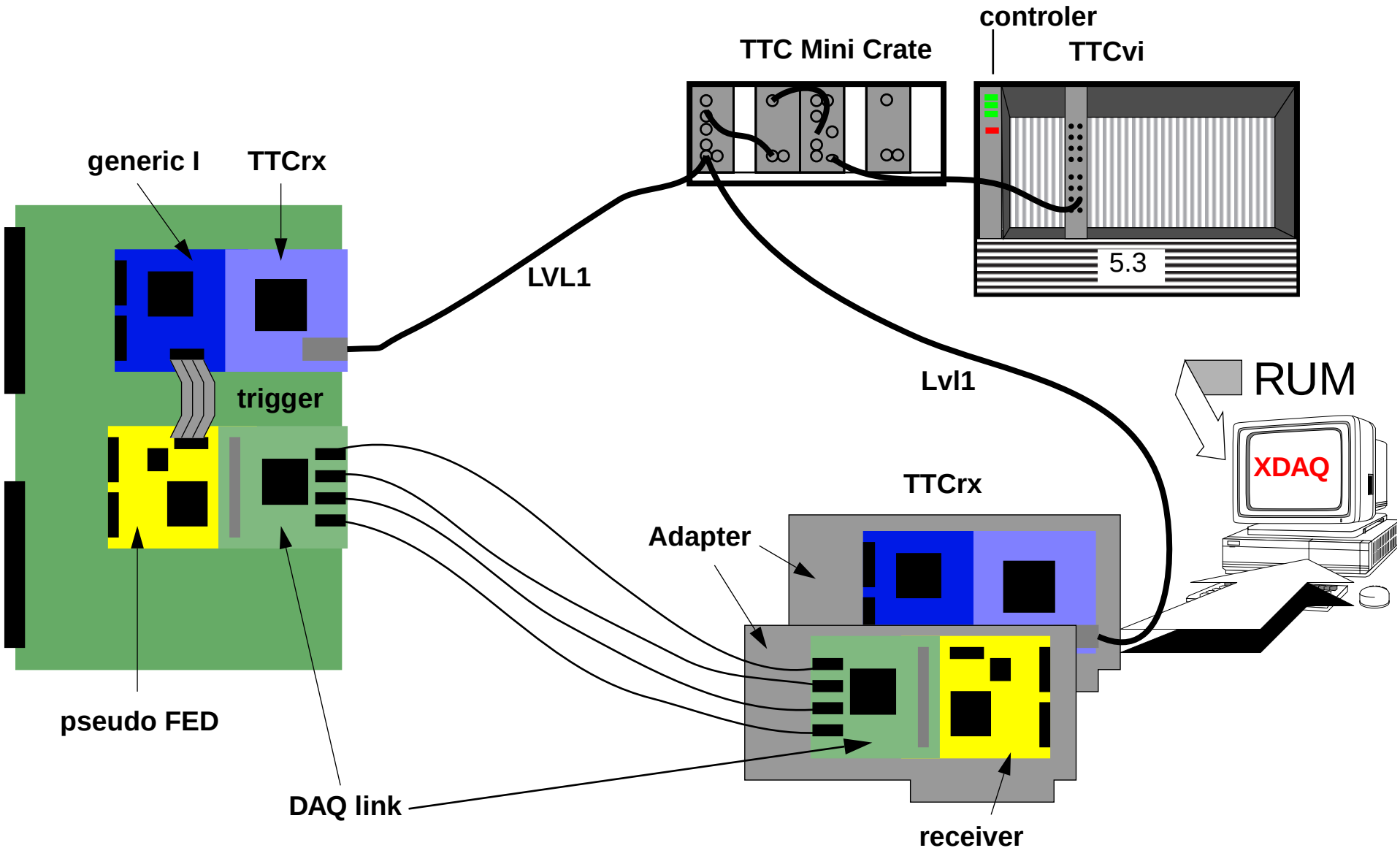
DAQ-Column Demonstrator

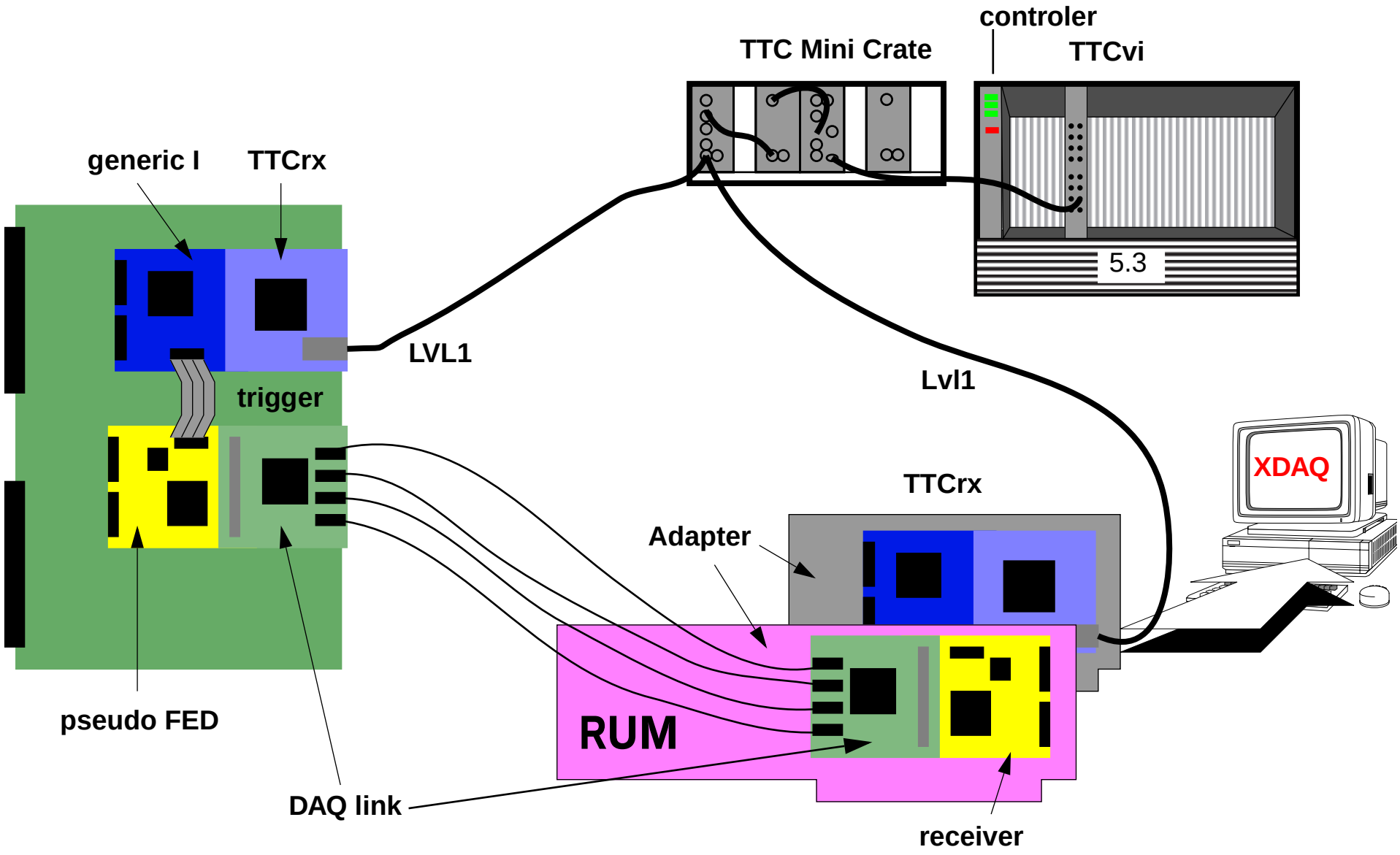
- Purpose
  - build a DAQ chain Pseudo-FED - RUM
  - demonstrate the concept
  - see for the first time bytes flowing between different building blocks
  - use software and hardware RUM
  - develop interface DAQ-Link RUM
  - identify bottlenecks in hard- and software
  - write results down into TDR
- NON-purpose
  - Performance and data throughput



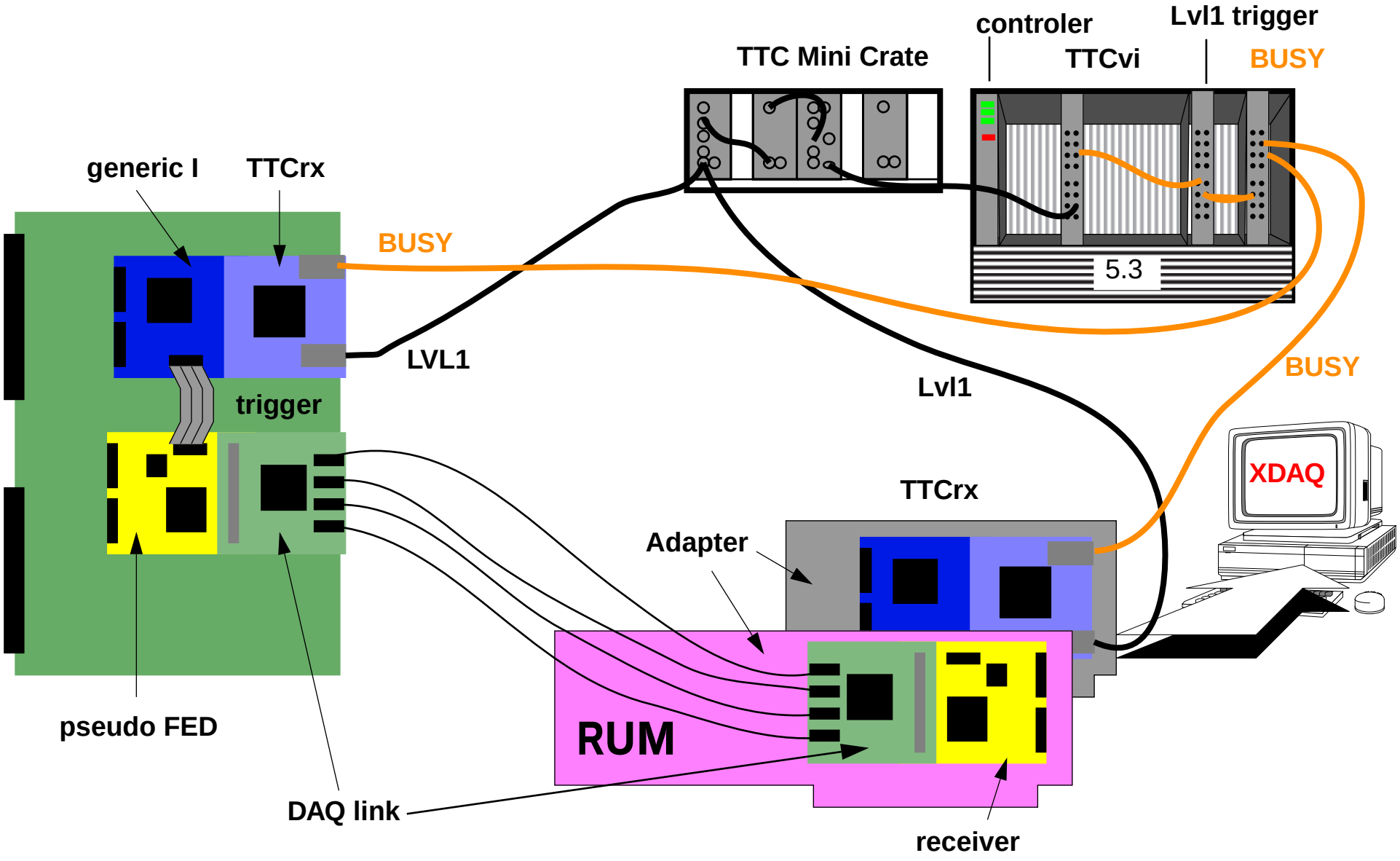
DAQ Column with Software RUM



DAQ clolumn with Hardware RUM

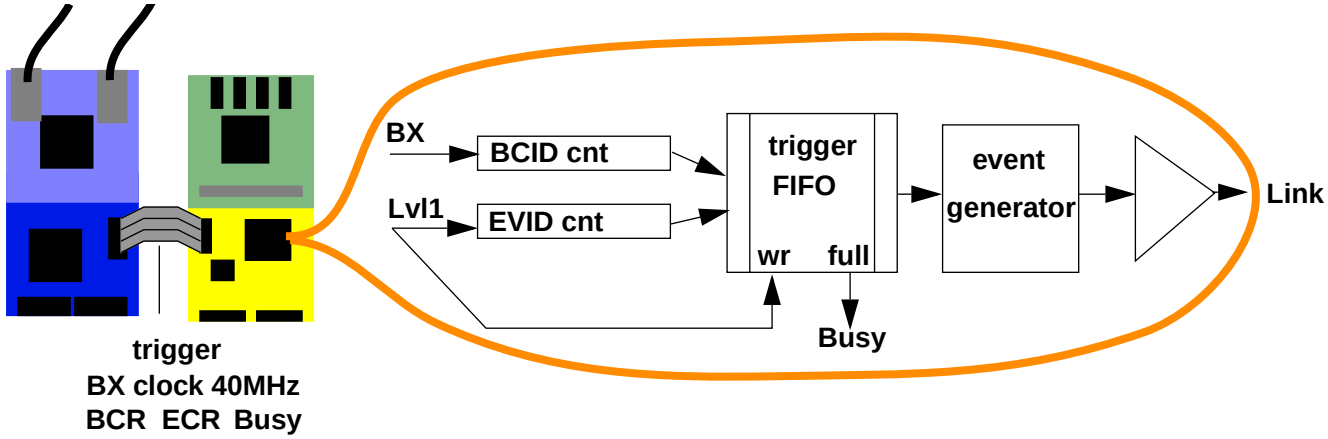


Implementation of BUSY

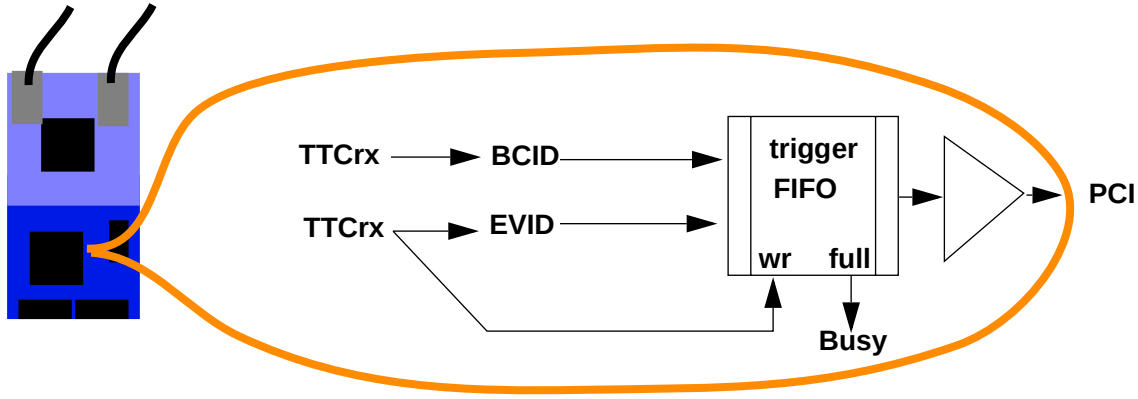


Trigger Receiver Board

- At pseudo FED:



- In RM (PC, XDAQ):



DAQ-Link Hybrid

- Two roles
  - FED / Sender

  receive triggers
  generate dummy data
  transfer them to the link
  - Receiver / Interface to RUM

  receive data from link in buffer fifo
  DMA to SDRAM
  setup descriptors for RUM
  interface to RUM (hardware / software)
- Status
  - Interrface RU-RUM defined
  - Receiver FPGA code exists (tested with Xilinx-Micky-Mouse simulator) for software RUM
    To be tested in Generic II
  - Pseudo FED to be done