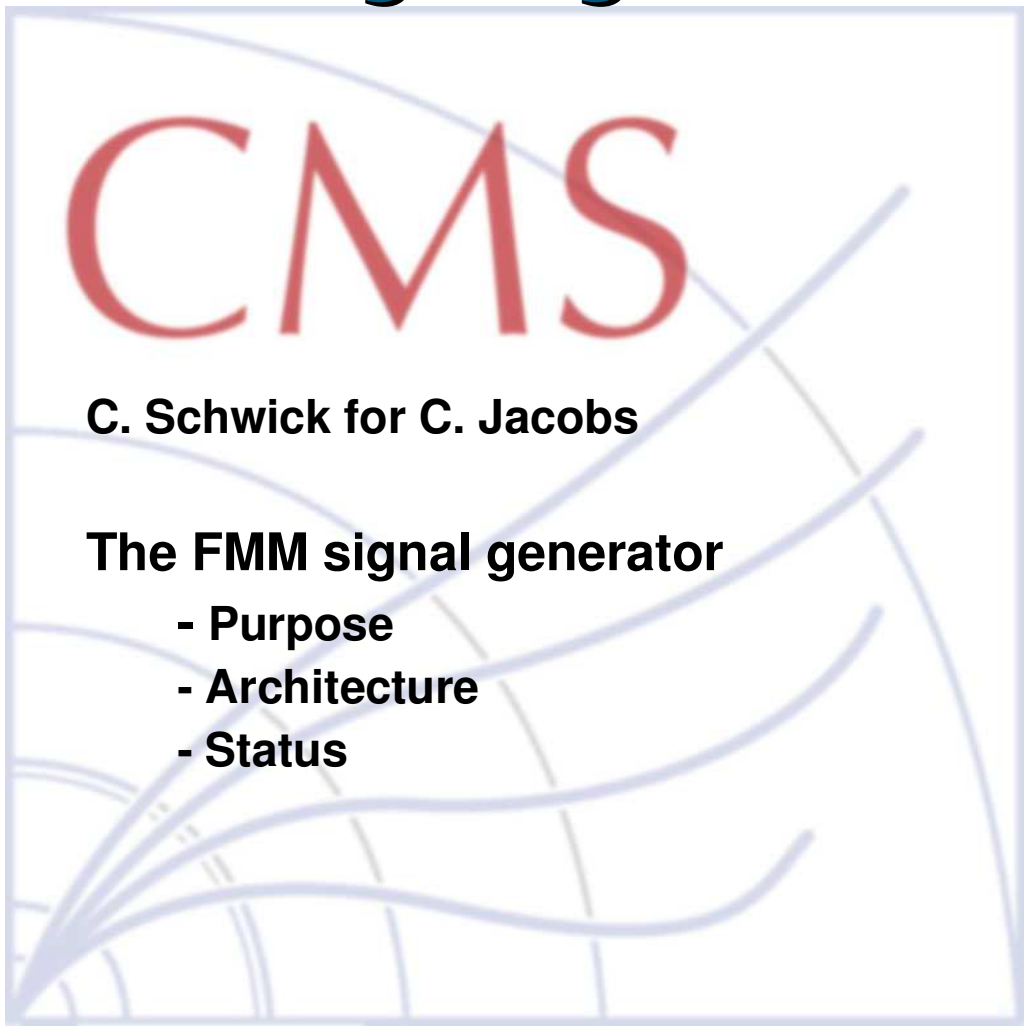
FFM signal generator



C. Schwick for C. Jacobs

The FMM signal generator

- Purpose
- Architecture
- Status

Introduction

- Need for a FMM signal generator:
  - To test the FMM
    - Needs some intelligence
    - Needs to generate all possible FMM signals
  - In TDRDemonstrator
    - Convert the simple backpressure signal into a busy signal
    - Needs no intelligence
    - Need 32 channels for PseudoFEDs
  - Detector groups
    - Might want to have a module to generate FMM signals before the final FED version is available?

Status

- PCB layout is under development
- Boards needed :
  - 2 for FMM testing
  - 2 for TDRDemonstrator:
    - 1 for the 32 PseudoFEDs
  - 1 to build a mini FMM to merge with the signals of the FRL crates

- Cost estimate per module
  - 1250 CHF per module (including 1U case, power supply)

- Production:
  - 15 PCB-boards
  - Production of 5 full modules
  - Additional production on request of subdetector groups.

GIII & Fedkit & SLINK

- Fedkit : new since last review
  - Mode of operations
  - Native driver
  - Number of GIIIs / Fedkits in CMS (table group, number of GIIIs, application)
  - FEDkit in testbeam: Tracker (L. Mirabito), HCAL (C.Tully)
  - Possibility to read out a FIFO with data received (without fedkit software)
- SLINK (final version for experiment):
  - Test initiated from receiver (FRL) side
  - New connector (better mechanics) (not for GIII test – kit version)
- Cables:
  - Test 3M ("inferior" quality): 5m cable 19 days (24h) (data generator 66 MHz / 64bit, link 80MHz)
    (10 m /15 m) since 22.08. (link 60 / 40 MHz)
  - One cable was broken (TDRDemonstrator) (no complaints from fedkit users, yet)
  - News on cable path in control room (Attila)

FED emulator

- Purpose
  - Use in TDR-Demo as data source (introduce TDR-Demo if first talk)
  - Use in test benches for preseries and full production
- Features
  - Implemented in GIII
  - 14 cards available for TDR demonstrator
  - Up to 256k event descriptors of 4 32 bit words
  - Event descriptor:
    - Length, source, seed, bx
    - delay to next event (for each event)
    - Trigger number can be chosen from counter or from descriptor for each event individually (makes it possible to generate synch-errors)
    - Software trigger or trigger on TTL signal
    - Backpressure generation (TTL signal)
    - Preload of 24 bit trigger counter
    - DAQ-active switch (on/off)

GTP emulator

- Purpose
  - In test benches
    - Realistic trigger distribution
    - Development of interface to GTL (data record)
    - Development of EVM details (path of trigger data to events in all partitions)
  - In final system
- Features
  - Implemented with GIII and SLINK
  - Functional description (wait for mail of Theo)

FRL final design

- Prototype available (photo)
- Context in system and main functionality (FEDbuider routing)
- Functional details
  - Block diagram
  - PCI layout of board
  - PCI-X technology for data transfer
  - Multiple firmware in flash
  - Receiver / merger card
  - Spy memory
  - Fedkit functionality
  - Event generator functionality
  - Crate layout with special purpose bus for trigger, backpressure (FMM)
- Test modes of FRL test bench
  - Description of test and what it tests
  - Results of tests done so far

Contd.: FRL

- Serial production (and preseries production) of FRL
  - Firmware tracking: automatic firmware Id generation in FPGA (also for GIII firmware)
  - Serial number for each board
  - Production of FRL series scheduled so far
    - 15.9. : 70 PCB
    - 15.10 : 10 cards with components
    - 15.11 : 60 more cards (if test of october cards go right)
  - Test system to be built for series: cable, electrical test (PCBs, adapter cards, connectors), burn in. NO full functionality test.
  - Production database
  - Test system : Layout of software and hardware is under development.

Trigger Distributor (Raphael)

- Purpose: Development card for Compact-PCI
  Use in CMS system:
  - Distribute trigger in FRL crate
  - Read “OR” of backpressure signal from FRLs
  - Interface to GTL emulator (and GTL)
  - Interface to FMM
- Generic Features
  - Contains 100 Mbit Ethernet
  - Nios Processor (50MHz) implemented in FPGA
  - Flash RAM (8 MB) and SRAM (4 MB)
  - Can function as Compact PCI controler
  - Several multi purpose connectors (LEMO, flat cable) for custom extensions
  - Firmware programmable LEDs

TTS-FMM

- Purpose and features
  - Review sTTS signals and their coding
  - Or of fast signals to generate backpressure
  - Keep history of state changes
  - Allow to search the or-tree
  - Allow to monitor deadtime of each aTTS participant
  - Clarify if this is feasable for emulator hardware produced by various subdetector groups
- Block diagram
- Next prototype
  - Faster readout via PCI
  - Larger FPGA to allow easy implementation of deadtime monitoring

Contd: FMM

- To be done (hardware)
  - Firmware to monitor deadtime of inputs
  - Hardware interface to TTS system for aTTS server
  - Hardware to test the full FMM
  - GIII add-on to generate FMM signals in test benches (under way)
  - Prototype II
- To be done (software)
  - Integration in TDRDemonstrator
  - Development of algorithms to monitor sTTS status of FEDs (deadtime histograms)

DAQ Column

- The DAQ-Column has been continued until end of last year
  - Update of measurements had been shown in TDR: goal of 200MB/s reached
  - Differences: EVM in 2-processor machine
  - Problem with slot-assignment in DELL: The 2 slots are not symmetric: The data throughputs depends on the slot assignment to the Myrinet card and the Fedkit.
  - Column is dead. (Parts are used for small stand-alone tests for hardware or driver development.) Now all measurements and tests are done in the TDR Demonstrator.