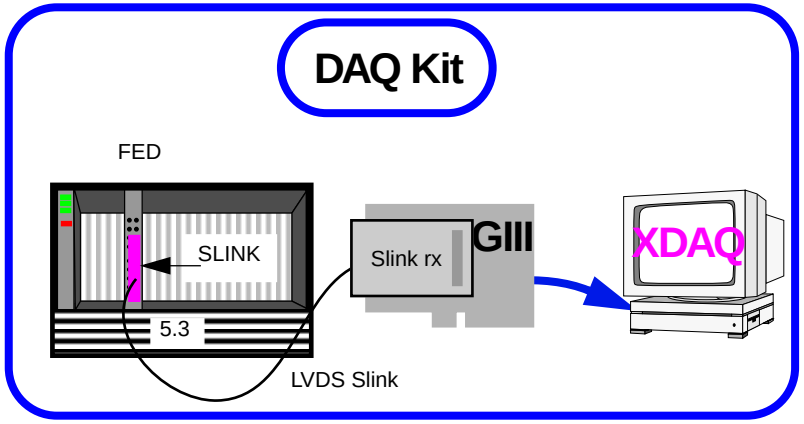
Test benches : plans

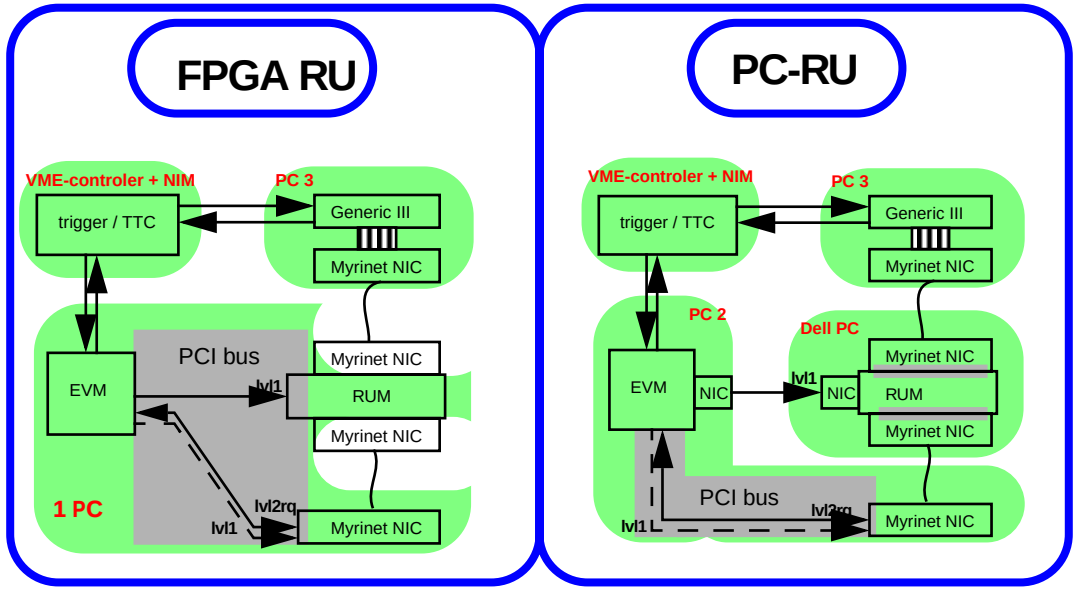
- Main test-benches
  - identification of the main benches
  - possible sub projects within the benches
- bench organization
  - material resources
    (what's needed in each bench)
  - where ?
    (laboratory space)
  - what and who ?
    (what are the activities, who could do it)

Test benches needed

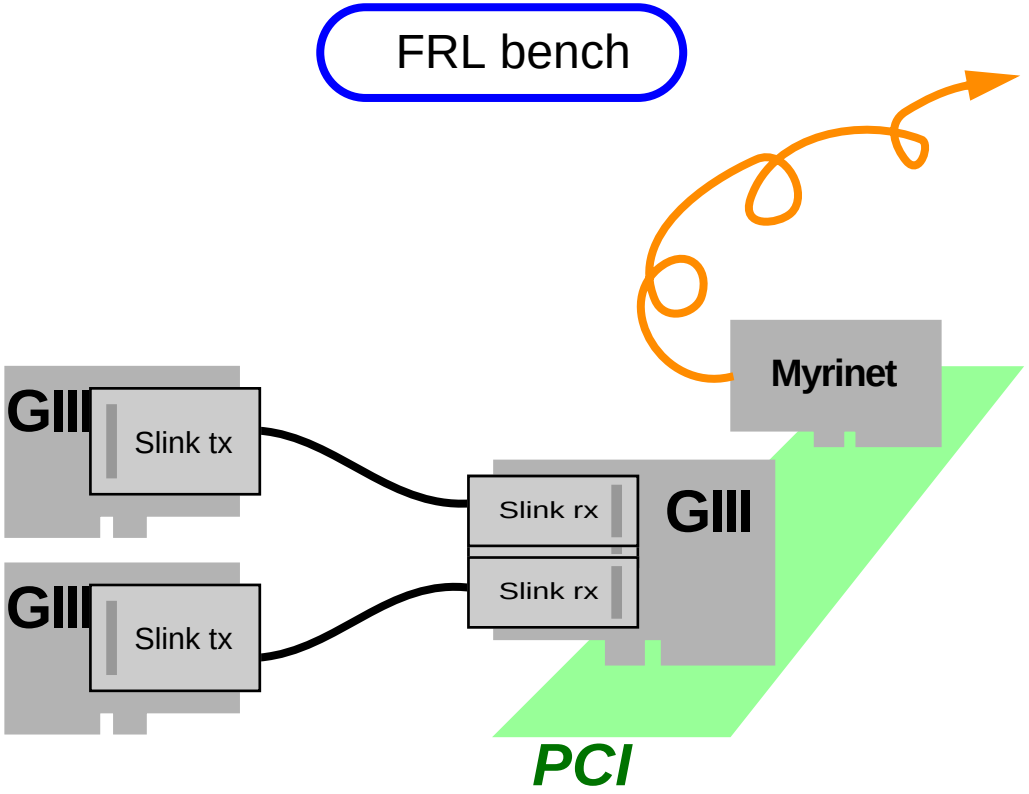
- "DAQ-Kit" bench
  - Package issued to collaboration to build local DAQ systems
  - CMS wide homogeneous DAQ environment



- RU bench
  - Test RU based on FPGA-RUM and RU based on PC-RUM in equivalent, realistic environment
  - try out different PCs for RU
  - compare both implementations



- FRL - bench
  - build an Slink (sender card with small FPGA, receiver with LVDS converters only)
  - build a merger
  - use GIII as FRL-intelligence



Not covered here : FED-builder and RU-builder benches
VME - PC interface test (could partly be done in connection with TTCvi usage)

Possible “add-ons” for the benches

- DAQ - KIT
  - Monitoring facility in GIII with NIOS processor
  - can be programmed by user :
    - histogramming,
    - checks on random samples,
    - detection of drifts in testbeam data
- RU - bench
  - Fancy data generator :
    - event size distributions downloadable in GIII (exists already in Dominique’s version),
    - generation random errors in header,
    - test bench for integrety codes
- FRL - bench
  - Fancy data generator (see above)
    - play systematically with worst case scenarios (one source a lot of data, the other only few data, different latencies for sources)
- Merge FRL-bench----RU-bench FRL-bench----FED Builder

Materiral resources

resource	DAQ - KIT	RU - bench	FRL - bench	Total
GIII	2 (1 datasource, 1“RUI-like”)	2 (1data generator (“FED”), TTCrx carrier (RM))	3 (2 data generator, 1 Merger)	7
PCs (PCI 64/66)	2 (1 soure, 1 receiver)	3 (software version) 1 RU (2 indep. PCI64/66) 1 EVM, 1 Data-Generator	2 (for in total 3 GII and one Myrinet card)	7
Myrinet cards	0	4 (2 links)	2 (one link ; later stage)	6
Slink sender	1	0	2	3
Slink receiver	1	0	2	3
Merger card	0	0	1	1
TTCvi sender setup	0	1	0	1
TTCrx	0	2 (EVM and pseudo FED)	0	2
others	trigger ?	trigger generator (GI, II, III, NIM ?)	trigger ?	

Task list

bench	task	who ?	months
DAQ - KIT	G III programming	Dominique	
	Slink Sender with FPGA	Dominique, Attila ?	
	Slink Receiver	Dominique	
	NIOS add-on	Dominique, Christoph	
	Protocol implementation	Luciano, Johannes	
	Control Software	Luciano, Johannes	
	Hardware Access	Eric, Christoph	
	XDAQ documentation	Lucaino, Johannes	
	XDAQ “toolkit - preparation”	Luciano, Johannes	

bench	task	who ?	months
RU b bench	pseudo FED, data format	Lucien, Attila?	
	Myrinet sender pseudo FED	Frans, Eric, Christoph?	
	Myrinet RUI	Frans, Eric, Christoph?	
	Myrinet RUO	Frans, Eric, Christoph?	
	Myrinet BU	Frans, Eric, Christoph?	
	EVM	Akos, Christoph?	
	Trigger setup	Akos ?	
	Column Control	Akos, Christoph?	
	RU software	Luciano, Johannes, Akos, Christoph	

bench	task	who ?	months
FRL - bench	Merger (hardware design)	Dominique	
	data generator	Lucien	
	trigger setup	Lucien, Dominique	
	GIII of Merger	Dominique, Attila	
	software	Eric?	

Please give your opinion:

Where do you want to be involved ?

Where don't you want to be involved ?

What other things are to do until the TDR submission ?