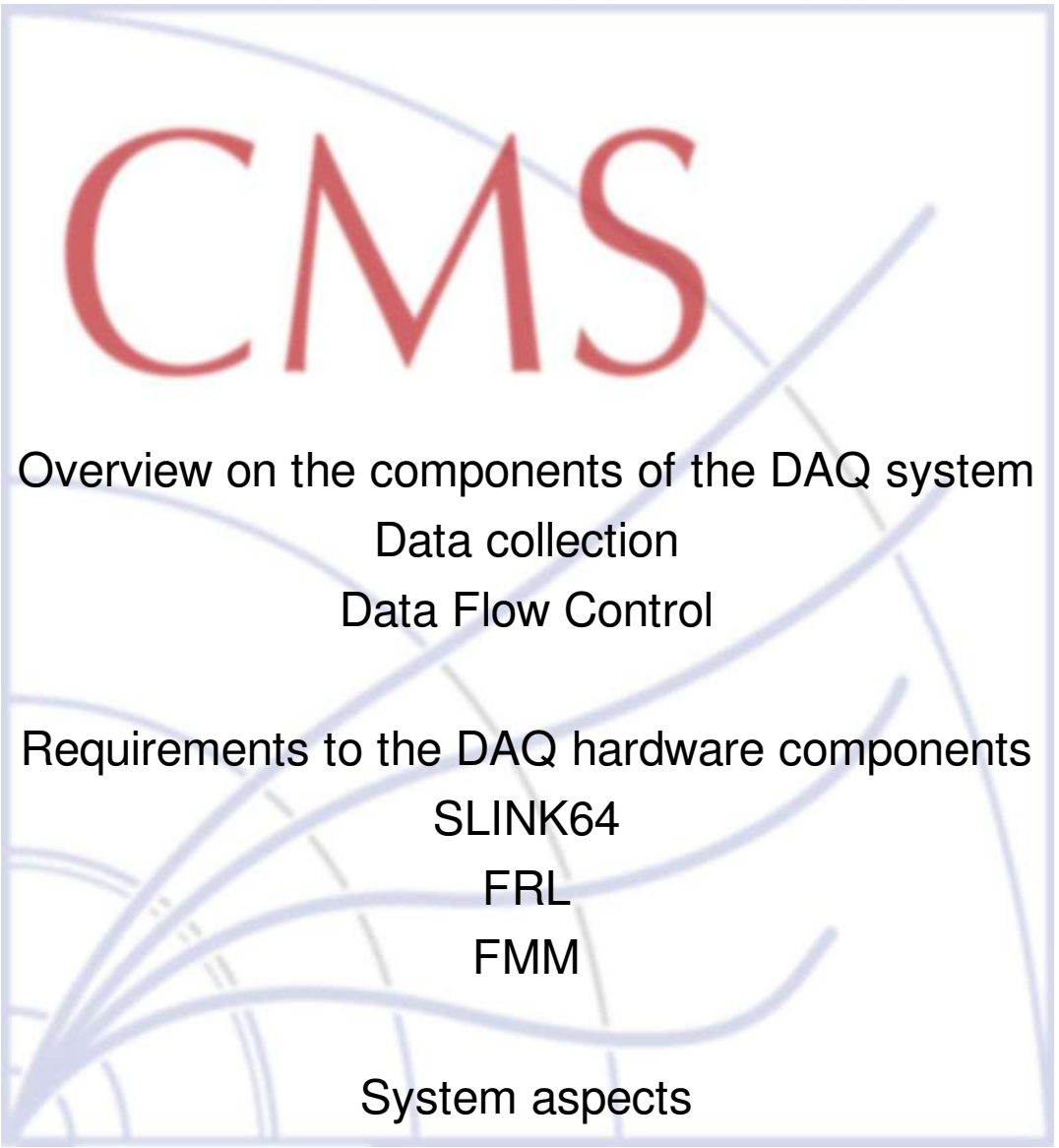
# TriDAS EDR
# Introduction and Overview




Overview on the components of the DAQ system

Data collection

Data Flow Control

Requirements to the DAQ hardware components

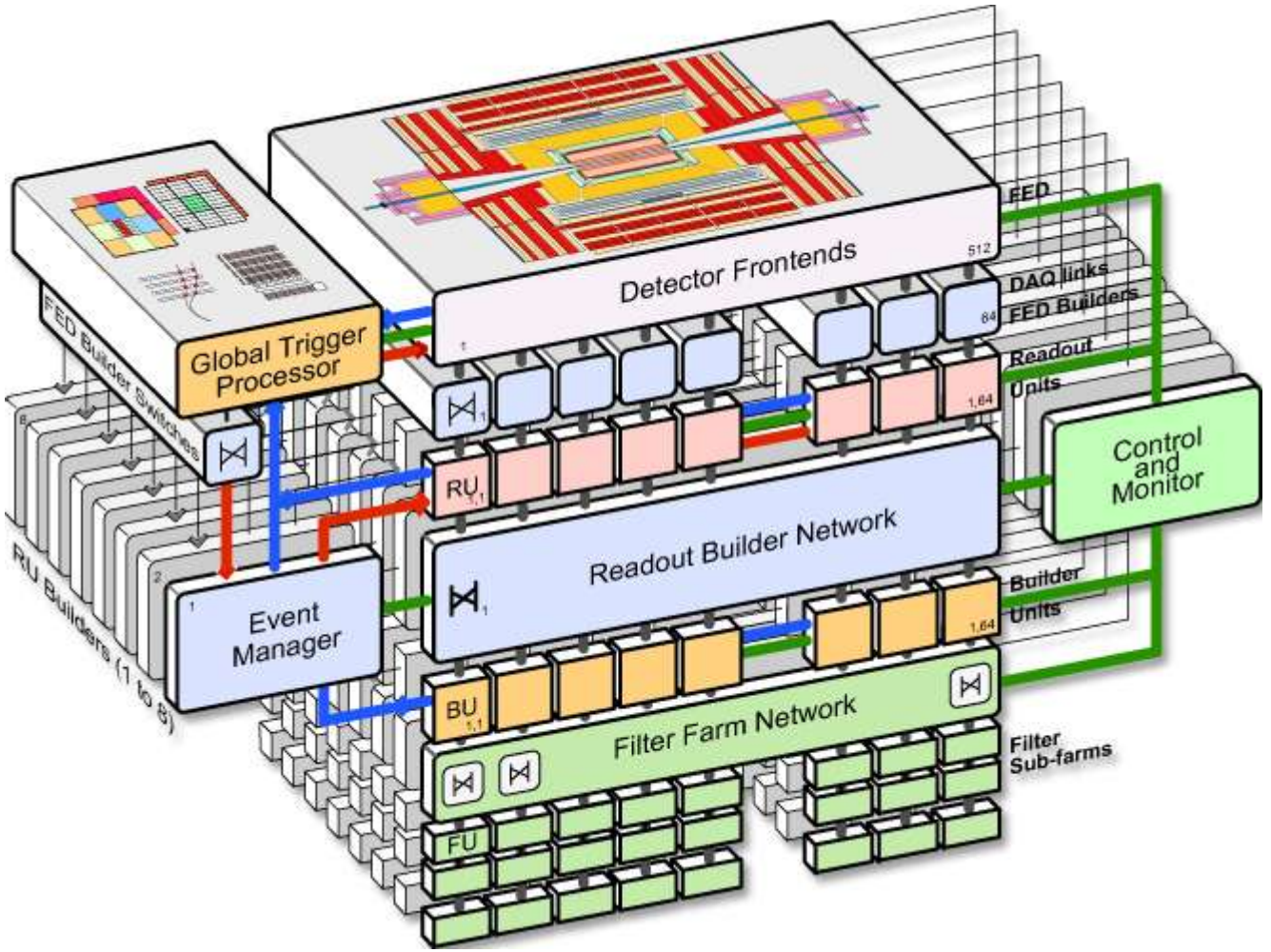
SLINK64

FRL

FMM

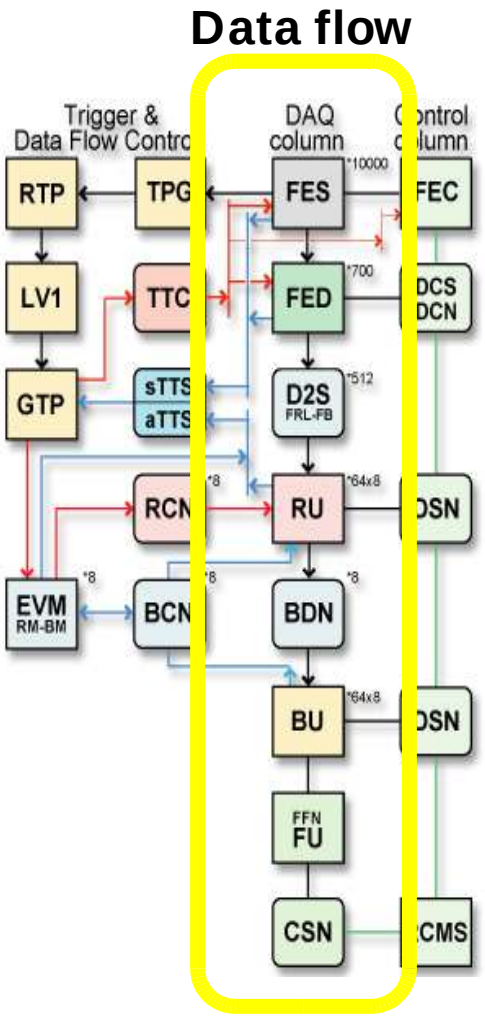
System aspects

# Overview on the CMS DAQ components



# Components of the DAQ system

- some numbers for Data flow:
  - 100 kHz Lvl1 rate
  - ?621? FEDs sources
  - FED: ca 2 kB / fragment
  - event size : 1 MB
- Data Flow Control (DFC)
  - avoid buffer overflows
  - avoid data corruption
  - 2 components : sTTS & sTTS

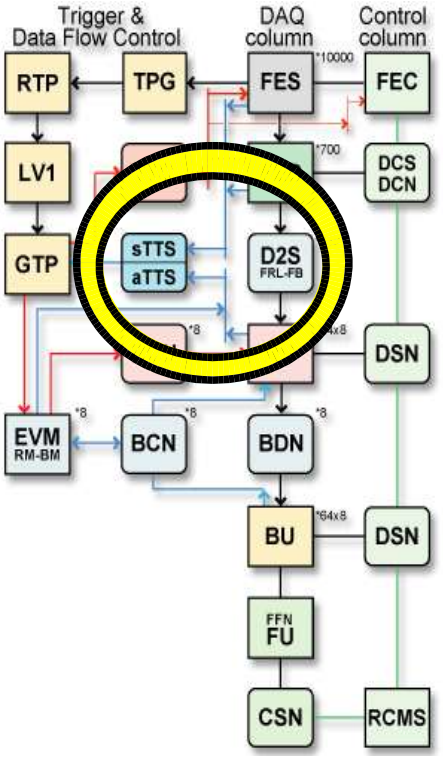



**Acronyms**

| | |
|---|---|
| BCN | Builder Control Network |
| BDN | Builder Data Network |
| BM | Builder Manager |
| BU | Builder Unit |
| CSN | Computing Service Network |
| DCS | Detector Control System |
| DCN | Detector Control Network |
| DSN | DAQ Service Network |
| D2S | Data to Surface |
| EVM | Event Manager |
| FB | FED Builder |
| FEC | Front-End Controller |
| FED | Front-End Driver |
| FES | Front-End System |
| FFN | Filter Farm Network |
| FRL | Front-End Readout Link |
| FS | Filter Subfarm |
| GTP | Global Trigger Processor |
| LV1 | Level-1 Trigger Processor |
| RTP | Regional Trigger Processor |
| RM | Readout Manager |
| RCN | Readout Control Network |
| RCMS | Run Control and Monitor System |
| RU | Readout Unit |
| TPG | Trigger Primitive Generator |
| TTC | Timing, Trigger and Control |
| sTTS | synchronous Trigger Throttle System |
| aTTS | asynchronous Trigger Throttle System |

# Components of the DAQ system

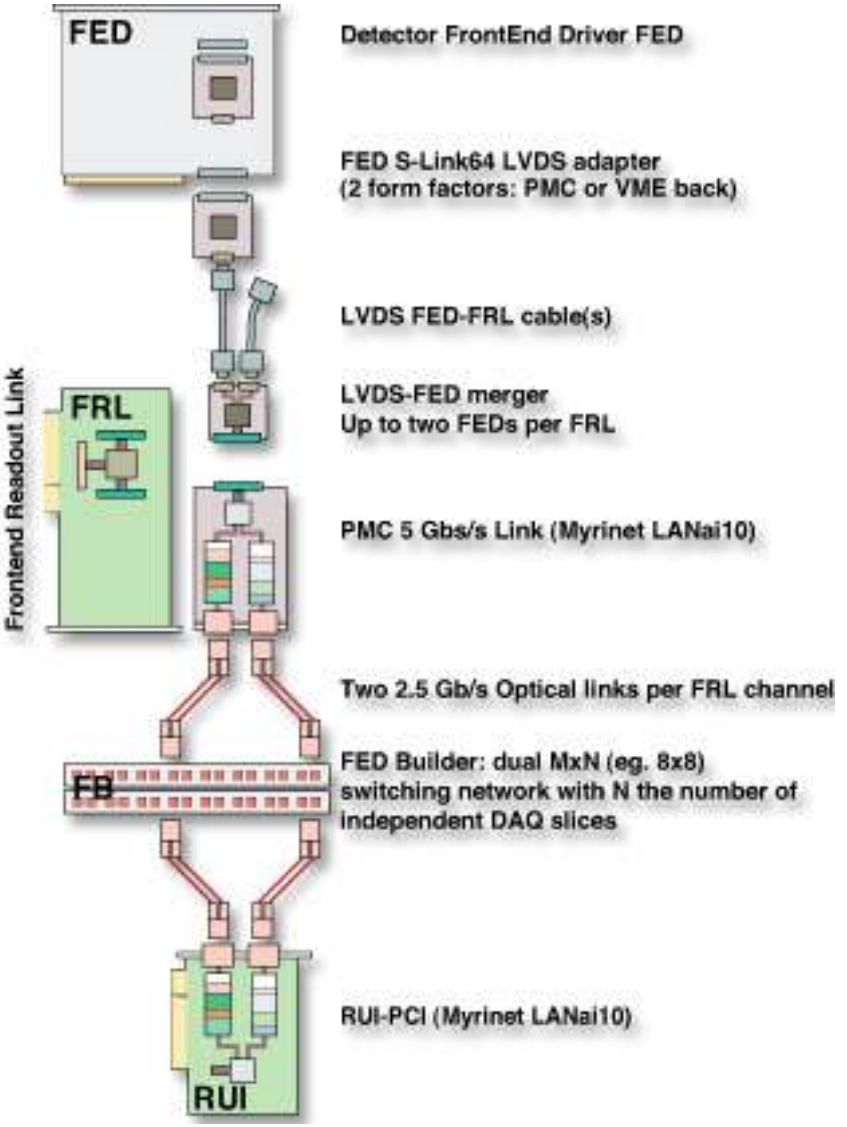
- custom hardware of DAQ system:
  - SLINK64 (FED-FRL connection)
  - FRL
  - sTTS Fast Merging Module (FMM)



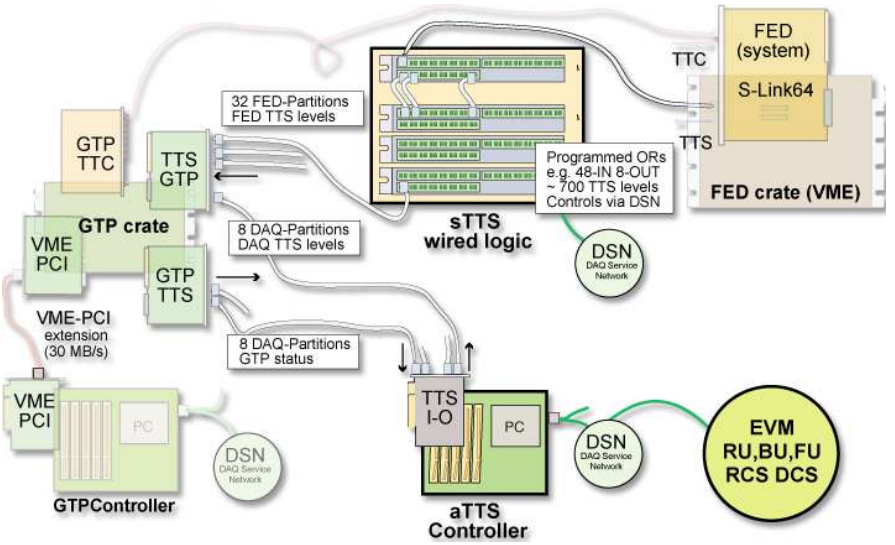

**Acronyms**

| | |
|---|---|
| BCN | Builder Control Network |
| BDN | Builder Data Network |
| BM | Builder Manager |
| BU | Builder Unit |
| CSN | Computing Service Network |
| DCS | Detector Control System |
| DCN | Detector Control Network |
| DSN | DAQ Service Network |
| D2S | Data to Surface |
| EVM | Event Manager |
| FB | FED Builder |
| FEC | Front-End Controller |
| FED | Front-End Driver |
| FES | Front-End System |
| FFN | Filter Farm Network |
| FRL | Front-End Readout Link |
| FS | Filter Subfarm |
| GTP | Global Trigger Processor |
| LV1 | Level-1 Trigger Processor |
| RTP | Regional Trigger Processor |
| RM | Readout Manager |
| RCN | Readout Control Network |
| RCMS | Run Control and Monitor System |
| RU | Readout Unit |
| TPG | Trigger Primitive Generator |
| TTC | Timing, Trigger and Control |
| sTTS | synchronous Trigger Throttle System |
| aTTS | asynchronous Trigger Throttle System |

# Details of the FED-DAQ connection



# Details of DFC system



# Requirements to the DAQ hardware

- SLINK64
- FRL
- FMM

# SLINK64 Requirements

Two groups of requirements addressing:

- Operation
- Testability

# SLINK64 requirements: operation

- Simple protocol for data input
  - FPGA driven
- sustained data throughput of 200MB/s
- peak data throughput of 400MB/s
  - to absorb fluctuations in data volume and/or trigger rate
  - to relax the requirements on buffer capacity of FEDs
- Implementation with 'plug-on' board
  - easy to exchange
  - flexibility for future upgrades

# cont'd: SLINK64 operational requirements

- full flow control
  - no data loss is allowed
- automatic link detection

- Requirement to FED: prepare data integrity test
  - CRC to be included in data trailer
  - CRC calculated on header, trailer and data payload
  - CRC has to be calculated by FED

# SLINK64 requirements: testability

- possibility to perform link test from receiver side (FED only needs to provide power)
  - tests the cable and connectors
  - tests electrical functionality of sender and receiver circuit

# FRL Requirements

Three groups of requirements addressing three domains:

- Operation
- Control and Monitoring
- Testability of DAQ system

# FRL Requirements: Operation

- Receive data from FEDs
  - Cope with maximal data transfer speed of 400 MB/s
- Merge data from up to 4 FEDs
- Limited buffer capability
  - to cope with momentary data rates > 200 MB/s
- Data integrity check (CRC)
  - flag corrupted events

# cont'd: operational requirements

- Format data fragments into fixed size buffers
  - necessary since DAQ is zero copy system working with chains fixed size buffers in order to avoid memory fragmentation.
- Feed data into FED builder
  - The FED builder input is a commercial Myrinet card (PCI-X)
- Allow readout of FEDs with local DAQ system
  - local FRL DAQ: allows to readout the CMS detector at low rate (several 100 Hz)
  - works independent main event builder

# FRL Requirements: Control and Monitoring

- Configuration of FED builder
  - i.e. must allow host computer access to Myrinet card
- Monitoring the status of the FED Builder
  - i.e. must allow host computer access to Myrinet car during data taking operation
- Allow to “spy” event fragments over PCI locally
- Allow statistical monitoring of quantities like event fragment sizes
  - simple histogramming facility

# FRL Requirements: testability of the DAQ system

- FRL must be able to perform SLINK64 test.
- FRL should allow to test the “down stream” DAQ system.
  - Allows DAQ testing independent of FED data.
  - Dummy event-fragment generation at full speed (2 kB fragments at 200 MHz/sec)
  - Playback of “real” (MC) event fragments in system to test the whole chain from the FED Builder to the Filter Farm
  - Needs some dummy trigger system
  - Needs some dummy data flow control system

# FMM requirements

Three groups of requirements addressing three domains:

- Operation
- Control and Monitoring
- Testability

# FMM requirements: Operation

- Collect sTTS status from all TTC partitions
- Merge sTTS status lines for each TTC  partition
  - Merging is done in a tree structure
  - result is one sTTS status for each TTC partition
  - result is transferred to the Trigger Controller System (TCS)
- The latency of the FMM system must be small enough to avoid buffer overflows in the FED and FE systems.
  - This requirement is valid for those sub-detectors which do not have an FE emulator in the trigger system.
  - ?? It is assumed that after a busy signal the FED system can accept still a few (up to 3) triggers.??

# cont'd: FMM operational requirements

- The FMM system should have a record of the status history for all of its inputs.
  - Status changes should be recorded with a time tag.
  - This allows “post-mortem” analysis.
- The FMM should allow to monitor the dead-time caused by every FED.
  - Needed to monitor the data flow and to trace problems.
  - The FMM is the only module which can perform this task.

# cont'd: FMM operational requirements

- The FMM must cope with the maximal expected state change rates.
  - State changes only occur in exceptional situations.
  - During normal operation state changes are expected to be less than 100Hz.
  - The FMM should also cope with higher pathological rates. (O10kHz).
- Monitoring applications should be able to obtain a continuous history of the status of each FED.
- The FMM should also be usable as interface of the aTTS system to the Trigger system.
  - In this case the FMM needs to have one sTTS input and one output for each possible DAQ partition (8).

# FMM requirements: Testability

- The FMM modules must be testable independent of the FEDs connected to its inputs.
  - The test should allow to verify the full electrical functionality of the board.

# System aspects

- Technology choice
  - Power supplies
- Grounding of the FRL system
- Spares

# Form factor and choice of technology

- FRL will be implemented as Compact PCI module
  - FRL needs higher data throughput than standard VME can provide (for local FRL DAQ mode)
  - Easy integration into PC based DAQ system based on zero copy data transfer.
    - allows to reuse software components and concepts developed for the Fedkit and the RU builder.
- FMM will be implemented as Compact PCI module
  - high data throughput in order to cope with pathologically high status transition rates
  - reuse of FRL PCI interface
  - reuse of existing software developments (FED-Kit)

# Power supply of Compact PCI crate

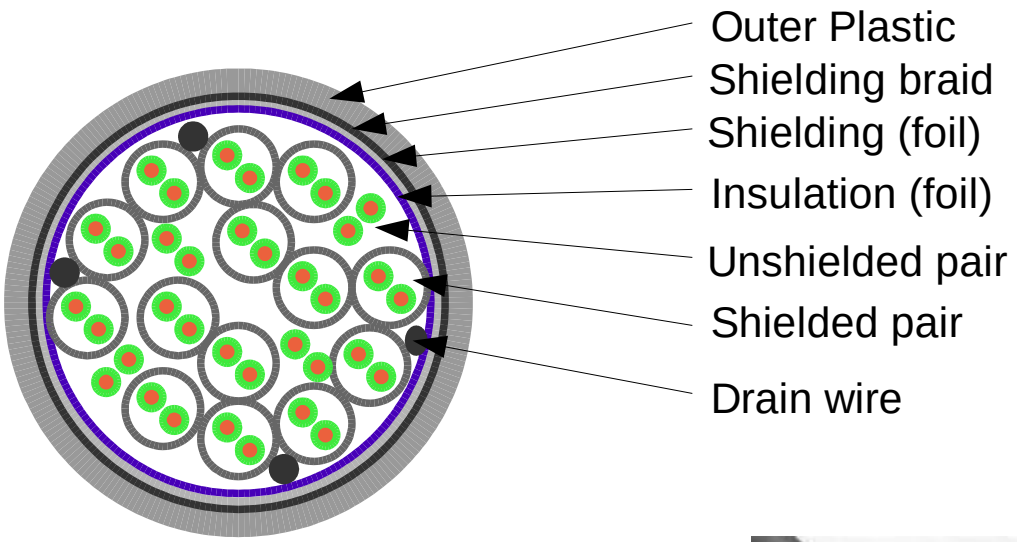
- 16 FRLs + 1 Trigger distributor will be housed in one Compact PCI crate.
- One FRL crate will consume ca. 400W.
- 32 FRL crates will be installed in USC55.
- Power supply (see EDMS for details):
  - 2 options for input
    - AC 220V  mains
    - DC 36V – 75V
  - ??? Remote enable / disable (on / off functionality of crate)???
  - Remote status control for all voltages (via Trigger distributor)

# cont'd: Power supply of Compact PCI crate

- 2 options for equipping a crate
  - 2 units with 250W each
  - 3 units with 200 W each (allows for 'hot-swap')

# Grounding of the SLINK-FRL system

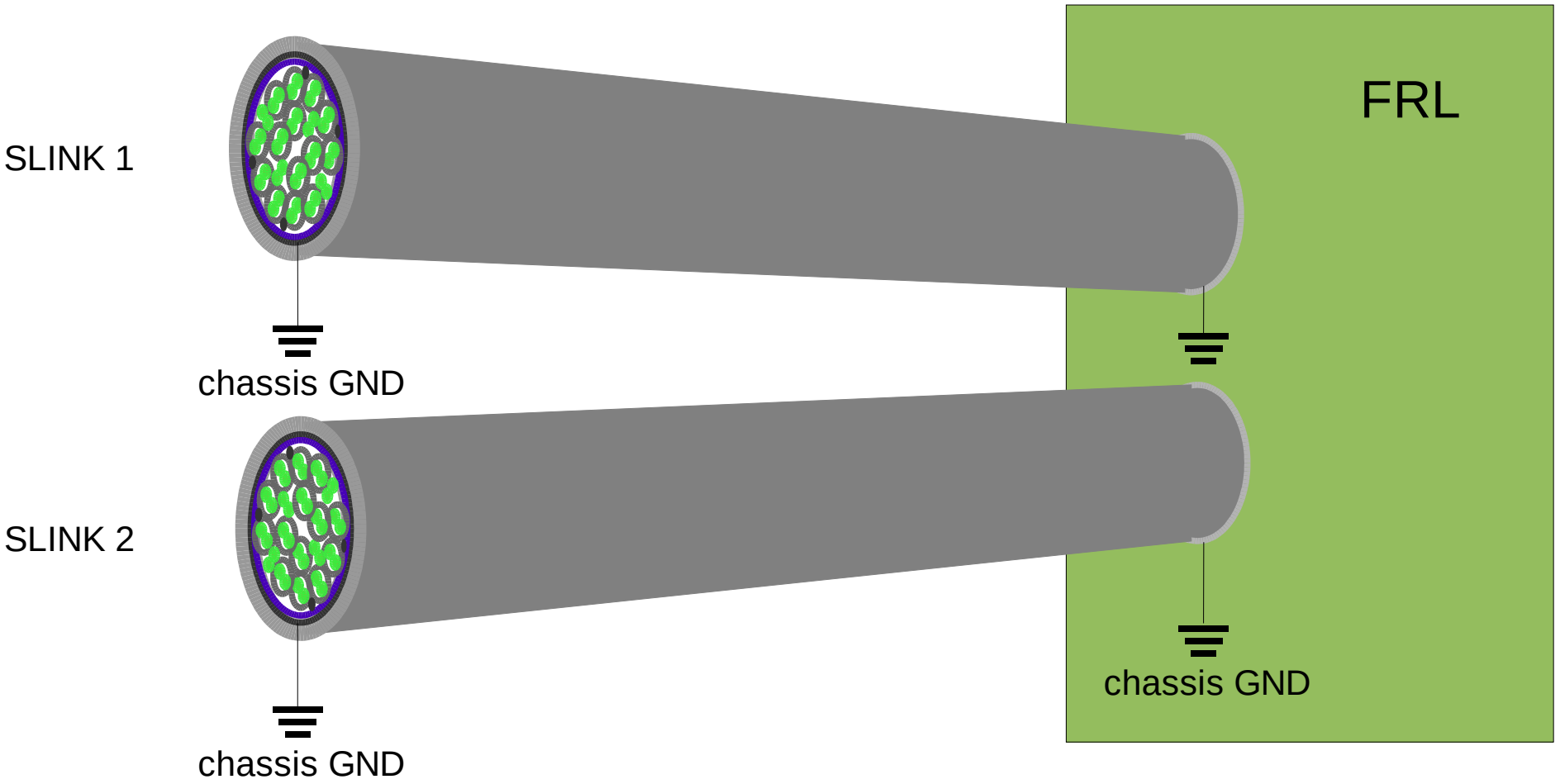
- The SLINK64 uses double shielded LVDS cables for data transmission:



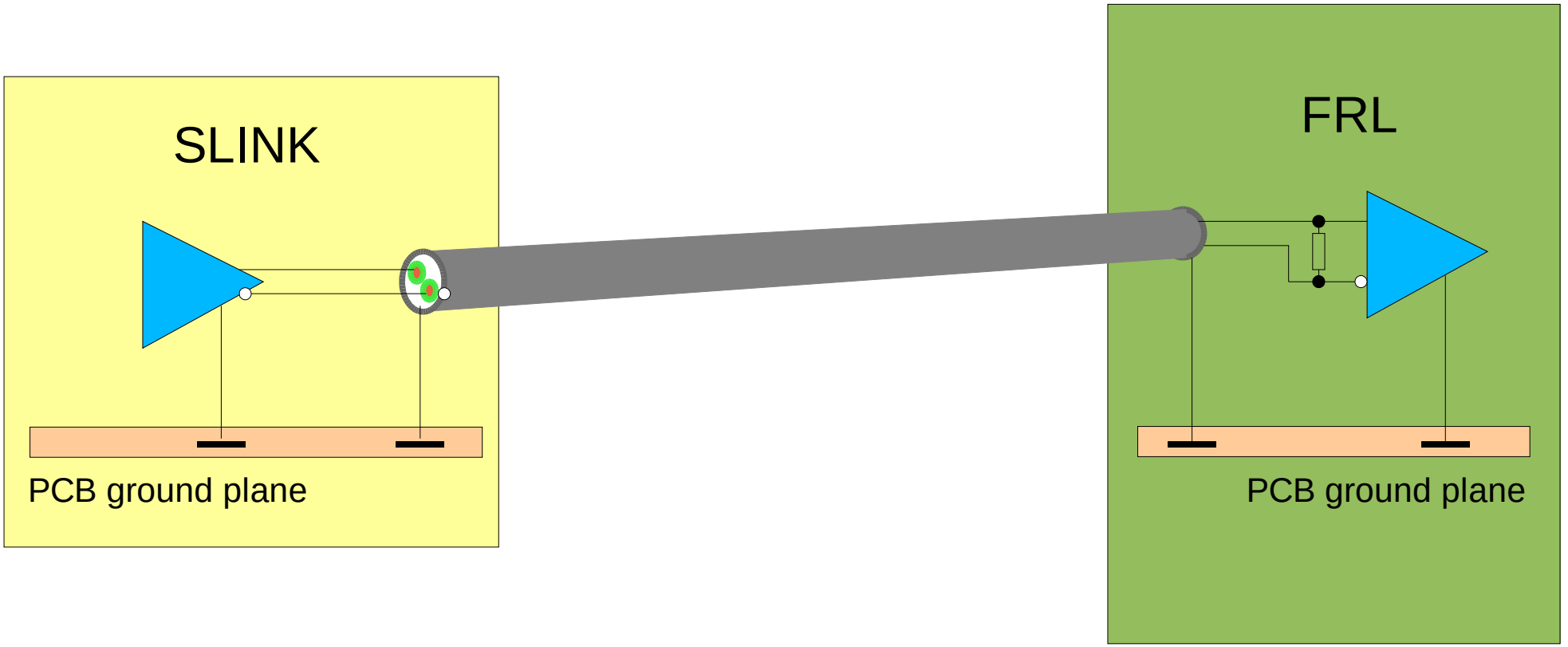

Unshielded cables are used for feedback signals from receiver to sender.

- Metal connector with with low inductance connection to outer cable shield

# LVDS cable grounding: outer shielding



# LVDS cable grounding: signal pair shielding



# 'Burn in' of the hardware

- Extensive testing of all produced boards will be performed for each produced module
  - see talk on test systems later
- Burn in of hardware will be done 'in place' after installation
  - All modules are easily accessible
  - After installation the modules will be operated continuously during DAQ commissioning.