Introducing the TTC Test and Monitoring Module

Prototype Issue 13/11/02

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This system aims to monitor all external signals delivered by a TTCRX chip. It couples physically to the Universal PCI Board (Figure 1- page 2). It selectively records TTCRX L1trigger sequences, Broadcast, Individual Address Commands, internal registers content and data flow status information for subsequent readout through a Local Bus. The front-panel displays 8 I/O - TTL/NIM configurable LEMO connectors for external signalling; a provision of spare Local Bus signals remains available for supplementary functions. A single, J-tag programmable, PLD (Altera) performs all processing involving TTCRX/FRONT-PANEL/Local Bus interactivity (Figure 2 - page 2).

Capturing TTCRX signals proceeds at 40.08 MHz instantaneous frequency, through a 512 words FIFO as input buffer. The Local Bus protocol accepts up to 66 MHz sampling clock rate, hence supports up to 20 Mword s^{-1} (block transfer option) readout rate.

Testing two prototypes (see current specification pages 3-5) showed that all TTCRX functionalities respond as expected. Producing similar modules would necessitate minor hardware (PC board or hand-made) correction; estimated cost ≈ 1300 CHF per unit.

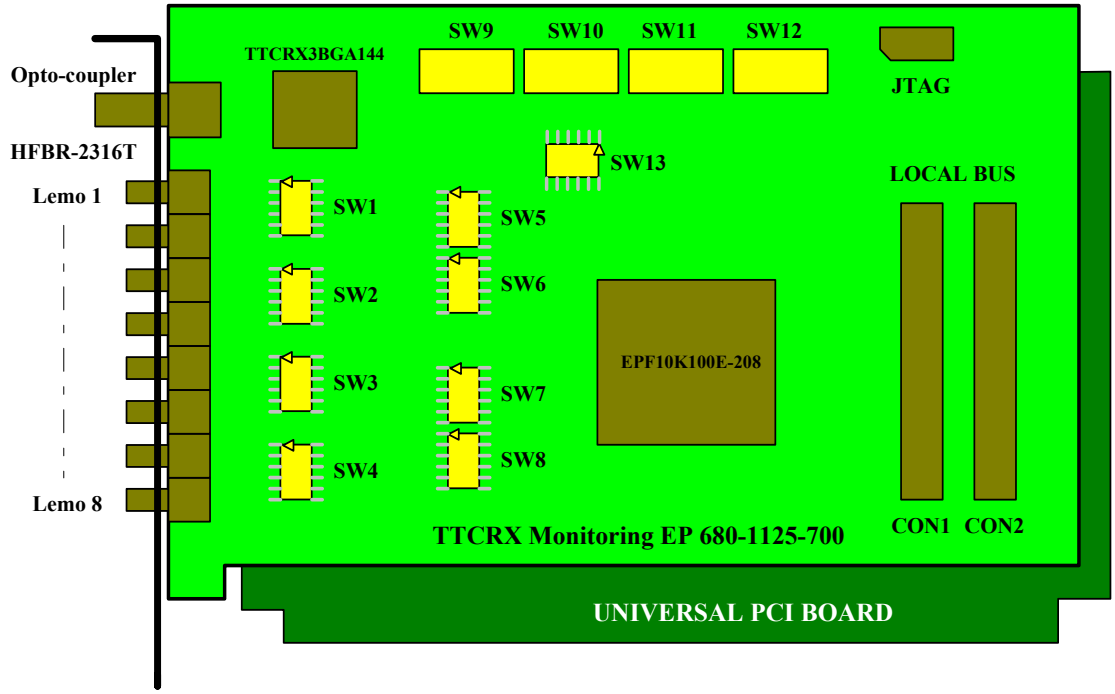


Figure 1 Physical Description

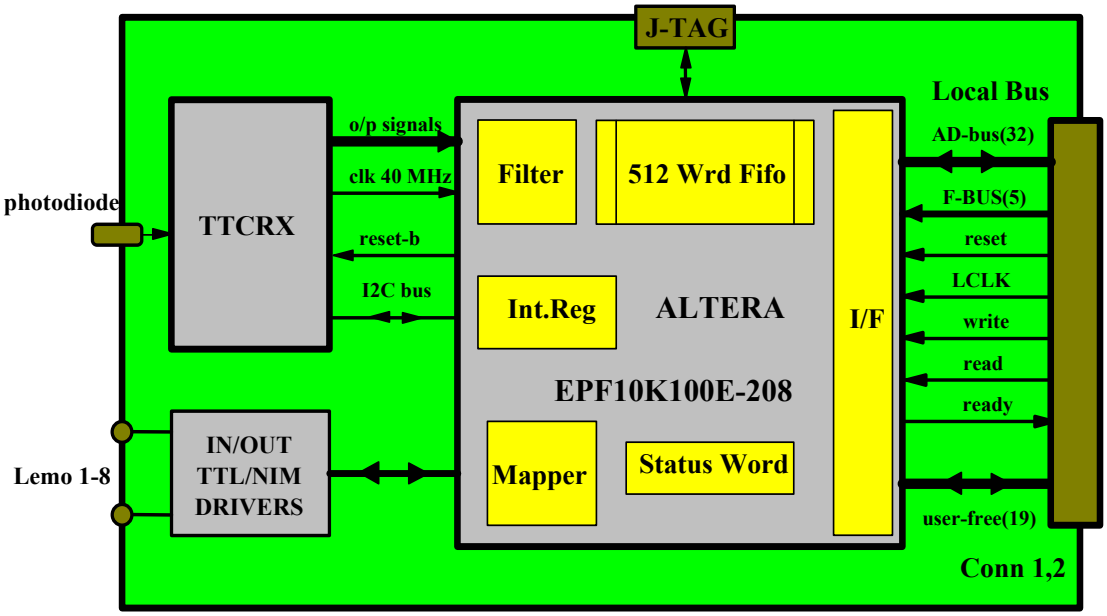
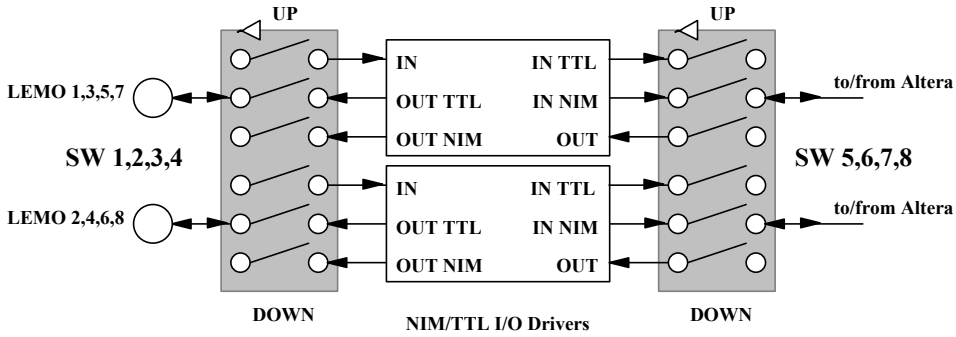


Figure 2 Topology

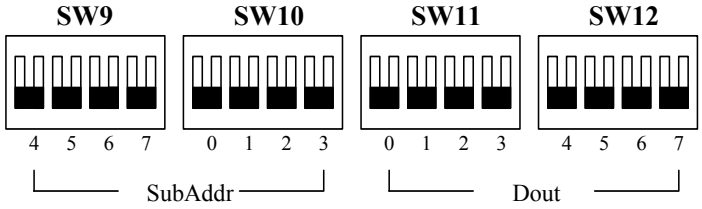
CURRENT SPECIFICATION

LEMO's CONFIGURATION SWITCHES

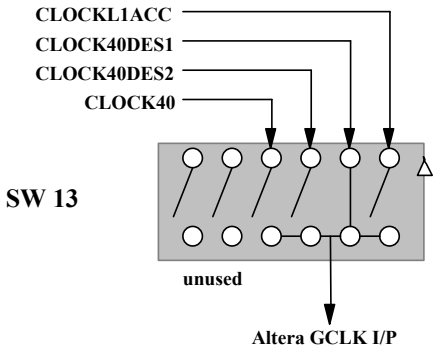


LEMO #	signal	direction	Switch #
1	clock40	out	1 up
2	L1A	out	1 down
3	EvCntRes	out	2 up
4	BCntRes	out	2 down
5	out_back-pressure	out	3 up
6	ext-back-pressure	in	3 down
7	daq enabled	out	4 up
8	ttcrxready	out	4 down

TTCRX IDENTIFIER



SELECTING THE TTCRX 40.08 Mhz SAMPLING CLOCK



Clock40des1 is the most probable choice.

Table 1 - FUNCTION ADDRESSES

Address Fbus[5:0]*	Direction	function
000000	write	Reset
000001	write	Select/Capture
000010	write	Busy
000001	read	Status
000000	read	Readout
010000	read	Block Transfer Readout
1rrrrr **	read	Read internal register

* Fbus[5:0] ⇒ user_free(2) & PCI_A/D_bus[12:8]
** rrrrr = Internal register number

Table 2 - BIT ASSIGNMENT: RESET & BUSY

data-bus	reset	Busy **
31:2	unused	unused
1	reset-b (ttcrx) *	unused
0	reset Altera	1= busy; 0 = not busy (latched)

* Reset-b time duration ≈ 50 μs.
** Two front-panel LEMO (*see Table 7*) reserved for back-pressure issue:
out back-pressure = FIFO backpressure ∪ *ext-backp*ressure ∪ *busy*.

Table 3 - BIT ASSIGNMENT: SELECT/CAPTURE

data-bus	Command word	comment
31:26	unused	
25	enable daq	1/0 = Start/stop capture *
24	enable iad	accept individual address data
23	enable brcst	accept broadcast data
22	enable L1A	accept L1A trigger
21:12	back pressure threshold[9:0]	warning against FIFO overflowing
11:0	unused	

* The content of the FIFO is cleared when enable daq is disasserted

Table 4 - BIT ASSIGNMENT: STATUS WORD

data-bus	status word	comment
31	Dberr	Straightforward TTCRX output
30	Sinerr	Straightforward TTCRX output
29	ttcrx ready	Straightforward TTCRX output
28	0	
27	back pressure	FIFO wordcount ≥ back-pres. threshold
26	fifo empty	
25	daq enabled	Reflects Select/Capture setting
24	iad enabled	Reflects Select/Capture setting
23	brcst enabled	Reflects Select/Capture setting
22	L1A enabled	Reflects Select/Capture setting
21:12	back pressure threshold[9:0]	Reflect Select/Capture setting
11	0	
10	fifo full	slow or late readout sequence, ignoring back-pressure feedback ?
9:0	fifo word count[9:0]	

Table 5 - BIT ASSIGNMENT: TTCRX DATA READOUT FORMAT

data-bus	L1A-first	L1A-second	Brcst	iad
31	1	1	0	0
30	1	0	1	0
29	0	0	0	1
28	0	0	0	0
27	ttcrx ready	ttcrx ready	ttcrx ready	ttcrx ready
26	fifo full	fifo full	fifo full	fifo full
25	back-pressure	back-pressure	back-pressure	back-pressure
24	fifo empty	fifo empty	fifo empty	fifo empty
23:20	0:0	evnt_cnter high[11:8]	0:0	0:0
19:12	0:0	evnt_cnter low[7:0]	0:0	SubAddr[7:4]
11:0	Bunch_cnter	evnt_cnter low[11:0]	Brcst[7:2] EvCntRes BCntRes	SubAddr[3:0] Dout[7:0] DQ[3:0]

Table 6 - BIT ASSIGNMENT: READ INTERNAL REGISTER

data-bus	register word
31:8	0:0
7:0	Register content